PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MPA-MIC/06/1940
Notification Date 07/18/2006

uPSD3400 Series Revision B - Part Number Change

MIC - MICROCONTROLLERS

Table 1. Change Identification

Product Identification (Product Family/Commercial Product)	uPSD3422, uPSD3433, uPSD3434, and uPSD3454
Type of change	Product design change
Reason for change	Fix known USB issues in silicon
Description of the change	see attached
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Part Number Change
Manufacturing Location(s)	

Table 2. Change Implementation Schedule

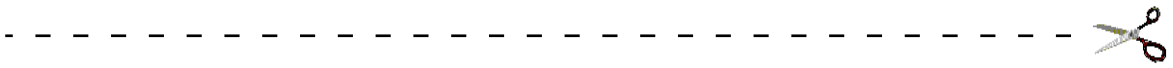
Forecasted implementation date for change	14-Jul-2006
Forecasted availabillity date of samples for customer	21-Aug-2006
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	14-Jul-2006
Estimated date of changed product first shipment	21-Aug-2006

Table 3. Change Responsibility

	Name	Signature	Date
Division Product Manager	Stephen Cheng		Jul.14 ,06
Division Q.A. Manager	Timothy Archer		Jul.14 ,06
Division Marketing Manager	Bryan Hahn		Jul.14 ,06

Table 4. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MPA-MIC/06/1940**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 07/18/2006**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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Subject: Product Termination Notice

Devices Affected: uPSD3422E/V, uPSD3433E/V, uPSD3434E/V and uPSD3454E/V

In order to fix a few of the known USB issues with the uPSD3400 series MCU die, it is necessary to implement a change to the MCU die for all uPSD3400 series devices. The new replacement uPSD3400 series devices are form, fit and functionally equivalent drop-in replacements for the corresponding part types. Please see the list below for a cross reference. For a simple cross to a device, simply replace the "-" with a letter "B" noting the revision level of the device.

The devices affected are listed below:

Old uPSD3400 series Part Numbers	New uPSD3400 series Part Number
uPSD3422EV-40U6	uPSD3422EVB40U6
uPSD3422E-40U6	uPSD3422EB40U6
uPSD3422EV-40T6	uPSD3422EVB40T6
uPSD3422E-40T6	uPSD3422EB40T6
uPSD3433EV-40U6	uPSD3433EVB40U6
uPSD3433E-40U6	uPSD3433EB40U6
uPSD3433EV-40T6	uPSD3433EVB40T6
uPSD3433E-40T6	uPSD3433EB40T6
uPSD3434EV-40U6	uPSD3434EVB40U6
uPSD3434E-40U6	uPSD3434EB40U6
uPSD3434EV-40T6	uPSD3434EVB40T6
uPSD3434E-40T6	uPSD3434EB40T6
uPSD3454EV-40U6	uPSD3454EVB40U6
uPSD3454E-40U6	uPSD3454EB40U6
uPSD3454EV-40T6	uPSD3454EVB40T6
uPSD3454E-40T6	uPSD3454EB40T6

Details of the changes that were made are available on the next several pages, in which the differences between the revision A and the revision B devices are noted.

Thank you,

STMicroelectronics
Microcontroller Division

34 Important notes

The following sections describe the limitations that apply to the uPSD34xx devices and the differences between revision A and B silicon.

34.1 USB interrupts with idle mode

Description

An interrupt generated by a USB related event does not bring the MCU out of idle mode for processing.

Impact On Application

Idle mode cannot be used with USB.

Workaround

Revision A - None identified at this time.

Revision B - Corrected in silicon so that a USB interrupt that occurs will bring the MCU out of idle mode.

34.2 USB Reset Interrupt

Description

When the MCU clock prescaler is set to a value other than $f_{MCU} = f_{OSC}$ (no division), a reset signal on the USB does not cause a USB interrupt to be generated.

Impact On Application

An MCU clock other than that equal to the frequency of the oscillator cannot be used.

Workaround

Revision A - The CPUPS field in the CCON0 register must be set to 000b (default after reset). The 3400 USB firmware examples set CCON0 register to 000b.

Revision B - Corrected in silicon so that when an MCU clock prescaler is used, a reset signal on the USB does generate an interrupt.

34.3 USB Reset

Description

A USB reset does not reset the USB SIE's registers.

Impact On Application

A USB reset does not reset the USB SIE's registers as does a power-on or hardware reset.

Workaround

Revision A and B - When a USB reset is detected, the USB SIE's registers must be initialized appropriately by the firmware. The 3400 USB firmware examples clear USB SIE's registers if USB reset is detected.

34.4 Data Toggle

Description

The data toggle bit is read only.

Impact On Application

The IN FIFO data toggle bit is controlled exclusively by the USB SIE; therefore, it is not possible to change the state of the data toggle bit by firmware.

Workaround

Revision A - For cases where the data toggle bit must be reset, such as after a Clear Feature/Stall request, sending the subsequent data on that endpoint twice results in getting the data toggle bit back to the state that it should be.

Revision B - A change in silicon was made so that the data toggle bit is reset by disabling and then enabling the respective endpoint's FIFO.

34.5 USB FIFO Accessibility

Description

The USB FIFO is only accessible by firmware and not by a JTAG debugger.

Impact On Application

Using a JTAG debugger, it is not possible to view the USB FIFO's contents in a memory dump window.

Workaround

Revision A and B - None identified at this time.

34.6 Erroneous Resend of Data Packet

Description

When a data packet is sent the respective IN FIFO busy bit is not automatically cleared by the USB SIE. This can cause a data packet to be erroneously resent to the host in response to an IN PID immediately after the first correct transmission of this data packet.

Impact On Application

Since the Data Toggle in the retransmitted data packet is toggled from when the data was first sent, the host will treat this packet as valid. If the identified workaround is not

implemented then this extra and unexpected data packet would result in a communication breakdown.

Workaround

Revision A and B - In the USB ISR, when an INx (x = the endpoint number of the IN FIFO) interrupt is detected, the IN FIFOs respective busy bit should be unconditionally cleared. The uPSD3400 USB firmware implements this workaround.

34.7 IN FIFO Pairing Operation

Description

When FIFO pairing is used on IN endpoints, an erroneous resend of a data packet may occur. See the "Erroneous Resend of Data Packet" note as it also applies when IN FIFO pairing is used.

Impact On Application

See the "Erroneous Resend of Data Packet" note as the impact is the same when IN FIFO pairing is used.

Workaround

Revision A and B - See the "Erroneous Resend of Data Packet" note as the workaround is the same when IN FIFO pairing is used.

34.8 OUT FIFO Pairing Operation

Description

When data packets are received from the host and FIFO pairing is used, the paired FIFOs may get out of order.

Impact On Application

The received data packets are read out of order compared to the way they were sent from the host. If the workaround is not implemented, the out of order packets would result in a communication breakdown.

Workaround

Revision A and B - In the USB ISR, when an OUTx (x = the endpoint number of the OUT FIFO) interrupt is detected, the OUT FIFOs respective busy bit should be unconditionally cleared. The uPSD3400 USB firmware implements this workaround.

34.9 Missing ACK to host retransmission of SETUP packet

Description

If a host does not properly receive the ACK (due to noise) from the uPSD3400 in response to a SETUP packet, it will resend the SETUP packet but the uPSD3400 will not respond with

an ACK. The host will resend the SETUP packet a number of times and if an ACK is not received from the uPSD3400, the host will issue a USB reset and then enumerate it again. Upon detecting a USB reset, the uPSD3400 firmware will reset and initialize the USB SIE putting the hardware back into the reset/initialized state so that when the next SETUP packet is received, the uPSD3400 will respond with an ACK to the host.

Impact On Application

If this occurs during enumeration, the impact is minimal as the host will retry the enumeration. If it happens after enumeration, the communication will break down between the host application and the uPSD3400 and will need to be re-established after the uPSD3400 is reset and enumerated again. In extremely noisy environments, the uPSD3400 may not communicate well over USB with the host application.

Workaround

Revision A and B - None identified at this time.

34.10 MCU JTAG ID

Description

MCU JTAG ID changed to differentiate revision A from revision B silicon through the JTAG port. The PSD JTAG ID remains the same.

Revision A MCU JTAG ID - 0x0451F041

Revision B MCU JTAG ID - 0x1451F041

Impact On Application

There will be no impact on the application. The impact will be to JTAG production programming equipment that may need to distinguish between revision A and B MCU silicon if the firmware is different depending on the revision level.

34.11 PORT 1 Not 5-volt IO Tolerant

Description

The port P1 is shared with the ADC module and as a result Port P1 is not 5V tolerant.

Impact On Application

5V devices should not be connected to port P1.

Workaround

Revision A and B - Peripherals or GPIO that require 5-Volt IO tolerance should be mapped to Port 3 or Port 4.

34.12 Incorrect Code Execution when Code Banks are Switched

Description

When a code bank is switched, the PFQ/BC contain values from the previously selected bank and are not automatically flushed and reloaded from the newly selected code bank.

Impact On Application.

Depending on the contents of the PFQ/BC when the code bank is switched, improper code execution may result.

Workaround.

The PFQ/BC must be flushed when the code bank is changed. Disabling and re-enabling the PFQ/BC will flush them. The following instructions are an example of how to flush the PFQ/BC:

```
ANL   BUSCON,#03Fh   ;Disable PFQ/BC
ORL   BUSCON,#0C0h   ;Enable PFQ/BC
```

Bank switching is typically handled by tool vendors in a file called l51_bank.a51. The uPSD tools offered by Keil and Raisonance now include an updated version of l51_bank.a51 for the uPSD products that flushes the PFQ/BC. The most recent banking examples available from ST's website include the updated l51_bank.a51 files.

34.13 9th Received Data Bit Corrupted in UART Modes 2 and 3

Description.

If the 9th transmit data bit is written by firmware into TB8 at the same time as a received 9th bit is being written by the hardware into RB8, RB8 is not correctly updated. This applies to both UART0 and UART1. Typically, the 9th data bit is used as a parity bit to check for data transmission errors on a byte by byte basis.

Impact on Application.

UART Modes 2 and 3 can't be used reliably in full-duplex mode.

Workaround.

Revision A and B - Some options include:

1. Only use Mode 1 (8 data bits) for full-duplex communication.
2. Use Mode 1 and a packet based communication protocol with a checksum or CRC to detect data transmission errors.
3. Use UART0 in mode 2 or 3 for transmitting data and UART1 in mode 2 or 3 for receiving data.
4. Use some form of handshaking to ensure that data is never transmitted and received simultaneously on a single UART configured in mode 2 or 3.

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