PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MPA-MIC/06/2202
Notification Date 12/19/2006

Qualification of Nantong Fujitsu (China) as an additional assembly site for lead free devices in PDIP 28 & PDIP 42 Shrink packages

MIC - MICROCONTROLLERS

Table 1. Change Identification

Product Identification (Product Family/Commercial Product)	All part numbers in PDIP 28 & PDIP 42 packages
Type of change	Package assembly location change
Reason for change	Closure of ST Malta PDIP 28 & PDIP 42 Shrink assembly line
Description of the change	MCD is pleased to announce the qualification of Nantong Fujitsu (China) assembly site for our lead free devices in PDIP 28 & PDIP 42 Shrink. Successful completion of the qualification plan as described page 4 will allow for production of the affected devices. There are no changes to the device design or part number as a result of this change.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Country of Origin : China
Manufacturing Location(s)	

Table 2. Change Implementation Schedule

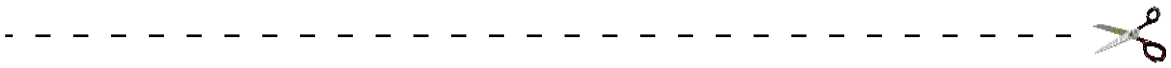
Forecasted implementation date for change	12-Mar-2007
Forecasted availabillity date of samples for customer	12-Mar-2007
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	12-Mar-2007
Estimated date of changed product first shipment	02-Apr-2007

Table 3. Change Responsibility

	Name	Signature	Date
Division Product Manager	J. Nicholas		Dec.15 ,06
Division Q.A. Manager	F. Demingo		Dec.15 ,06
Division Marketing Manager	Y. Benmokhtar		Dec.15 ,06

Table 4. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MPA-MIC/06/2202**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 12/19/2006**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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MCD Pkg06 13 QUALIFICATION PLAN

Qualification of :

PDIP 28,32S,42S in NFME (Nantung Fujitsu)

Qualification Reference : MCD Pkg06 13

Issued on : 12/8/2006

Assembly Plant : SC - NANTONG FUJITSU - CHINA
Assembly Line : PDIP Line
Package / Process : Pure Sn Plating

Scope :

Comment :

Test Vehicles :

RL Code	Number of Lots
F0T7*201XXX1	2
F076*801XXX1	2
F1D5*815XXX1	2

Test Vehicle Features:

Die information

Test Vehicle	TV 1	TV 2	TV 3
Rawline	F076*801XXX1	F0T7*201XXX1	F1D5*815XXX1
psfdescr	ST7LITE25x Flas	ST62E1X	ST72324J4 Flash
Wafer Fab	AMK 6'	AGRATE AG8 8'	PHOENIX 8'
FAB Process	CMOSM5S-F-DL	CMOSM5-E	CMOSM6D-FTP
Die BackSide	LAPPED SILICON	LAPPED SILICON	LAPPED SILICON
Passivation	USG + NitUV (HFP USG	USG + PSG + SiOn	PSG + NITRIDE
Die Step X	4645.00	2440.00	3450.00
Die Step Y	5180.00	3475.00	2985.00
Die Thickness	375	375	375
Pad Open X	90	90	90
Pad Open Y	90	90	90
Min Pad Pitch	150.00	150.00	150.00

Assembly information

Test Vehicle	TV 1	TV 2	TV 3
raw line	F076*801XXX1	F0T7*201XXX1	F1D5*815XXX1
Assembly Plant	NANTONG FUJITSU	NANTONG FUJITSU	NANTONG FUJITSU
Packaging	PDIP 32 .4 Cu .25 Shrink	PDIP 28 .6 Cu .25	PDIP 42 .6 Cu .25 SHRINK
POA	0123183	0016130	0042339
BSA	CD00145675 2.0	N/A A	N/A A
B/D	8029366 A		
Bond Placement	75% IN B.P.O.	75% IN B.P.O.	75% IN B.P.O.
FCA	7683721		
IEDB Flow	38819	10	10
Ecopack	E	E	E
E Mark	e3	e3	e3
2nd Level Interco	Sn	Sn	Sn
MSL	0	0	0
Peak Body Temp (C)	0	0	0
Frame/Substrat	FRAME FOR DIP32S 193X217		
D/A Material	CRM - 1033BF SUMITOMO EPOXY GLUE	CRM - 1033BF SUMITOMO EPOXY GLUE	CRM - 1033BF SUMITOMO EPOXY GLUE
M/C Material	SG8300SY SUMITOMO RESIN	SG8300SY SUMITOMO RESIN	SG8300SY SUMITOMO RESIN
Wire	GOLD WIRE-1 MIL DIAMETER	LF FOR DIPS 28L IN NANTUG FUJITSU 150MILS SQ	LF FOR DIP 42 IN NANTUNG FUJITSU 210 MILS SQ
Field15		GOLD WIRE-1 MIL DIAMETER	GOLD WIRE-1 MIL DIAMETER

Package Reliability Trials :

Reliability Trial		Test Conditions	Pass Criteria	Unit per Lot
TCT	JL3+Thermal Cycling MIL Std 883, Method 1010	-40°C, +150°C	500Cy,1000Cy	50
PPT	JL3+Pressure Pot	121°C, 100% RH, 2 Atm	240h	50
THS	JL3+Temperature Humidity Storage	85°C, 85% RH,Unbiased	500h,1000h	80
SAM	SAM analysis	Delamination check : Top, Bottom Through	@ T0,1000 Cy, 240h PPT	15

Construction Analysis

150 extra units/lot are needed for package construction analysis

Attachment : Reliability tests description

TEST NAME	DESCRIPTION	PURPOSE
JLn: **Jedec Level n surface mounting simulation**	The device is submitted to a typical temperature profile used for surface mounting, after controlled moisture absorption.	*As stand-alone test:* to investigate the level of moisture sensitivity. *As preconditioning before other reliability tests:* to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
TCT: **Temperature Cycles Test**	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, and die attach layer degradation.
PPT: **Pressure Pot Test**	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
HTS: **High Temperature Storage**	The device is stored in unbiased condition at the max. Temperature allowed by the package materials, sometimes higher than the max. Operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress voiding.
THS: **Temperature Humidity Storage**	The device is stored at controlled conditions of temperature and relative humidity.	To investigate failure mechanisms activated in the die-package environment by wet conditions. Typical failure mechanisms are corrosion and surface effects related to the molding compound.
TST: **Thermal Shock Test**	The device is submitted to cycle thermal shocks through alternate immersion in a hot and a cold oil bath.	To investigate failure modes related to the thermo mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moldings compound delamination, wire-bonds failure, die-attach layer degradation.

TEST NAME	DESCRIPTION	PURPOSE
THB: **Temperature Humidity Bias Test**	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To investigate failure mechanisms activated in the die-package environment by electrical field and wet conditions. Typical failure mechanisms are electrochemical corrosion and surface effects related to the moulding compound.
OLT: **Operating Life Test**	The device is stressed in dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature, load current, internal power dissipation.	To simulate the worst-case application stress conditions. The typical failure modes are related to electromigration, wire-bonds degradation, oxide faults.
ESD: **Electrostatic Discharge**	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models.	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU: **Latch-up**	The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effects inducing latch-up.

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