

# PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-SNV/07/2262 Notification Date 01/10/2007

# M24C04-R (1.8V to 5.5V Vcc range), 4Kbit Serial I†C Bus EEPROM Redesign and Die Optimization SNV - STANDARD MEMORY

#### **Table 1. Change Identification**

Product Identification (Product Family/Commercial Product)	M24C04 1.8V to 5.5V Vcc range
Type of change	Product design change
Reason for change	Production cap. increase & line up to state of the art of low volt. desig
Description of the change	New design
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Process Techno/Wafer fab id is "Q" for New design
Manufacturing Location(s)	

#### **Table 2. Change Implementation Schedule**

Forecasted implementation date for change	11-Mar-2007
Forecasted availability date of samples for customer	08-Jan-2007
Forecasted date for <b>STMicroelectronics</b> change Qualification Plan results availability	08-Jan-2007
Estimated date of changed product first shipment	11-Mar-2007

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**Table 3. Change Responsibility** 

	Name	Signature	Date
Division Product Manager	C. DARDANNE		Jan.08 ,07
Division Q.A. Manager	N. YACKOWLEW		Jan.08 ,07
Division Marketing Manager	B. RODRIGUES		Jan.08 ,07

#### **Table 4. List of Attachments**

Customer Part numbers list	
Qualification Plan results	

Customer Acknowledgement of Receipt	PCN MMS-SNV/07/2262
Please sign and return to STMicroelectronics	Sales Office Notification Date 01/10/2007
□ Qualification Plan Denied	Name:
□ Qualification Plan Approved	Title:
	Company:
□ Change Denied	Date:
□ Change Approved	Signature:
Remark	

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## PRODUCT / PROCESS CHANGE NOTIFICATION

## M24C04-R (1.8V to 5.5V Vcc range), 4Kbit Serial I<sup>2</sup>C Bus EEPROM Redesign and Die Optimization

#### What is the change?

The M24C04-R (Vcc 1.8V to 5.5V) 4 Kbit I²C bus Serial EEPROM device, processed in the CMOSF6SP/DM (Single Poly/Double Metal) 36% shrink Process Technology and currently produced in the ST AMK (Singapore) 6 inch wafer diffusion plant, will be redesigned for improved performances using the same Process Technology in the same wafer diffusion plant.

#### Why?

The STMicroelectronics Serial Non-Volatile Memories strategy is to support the growth of our customers on a long-term basis. In line with this commitment, the qualification of the redesigned M24C04 die in the same CMOSF6SP/DM Process Technology will increase the production capacity throughput, reduce the lead-time and consequently improve the service to our customers.

#### When?

The production of the new M24C04 in the ST AMK (Singapore) 6 inch wafer diffusion plant will ramp up from January 2007 and shipments will start from March 2007 onward.

The phase out of the current version of the M24C04 will start from March 2007 with a completion planned for June 2007.

#### How will the change be qualified?

The new version of the M24C04 has been qualified using the standard ST Microelectronics Corporate Procedures for Quality and Reliability.

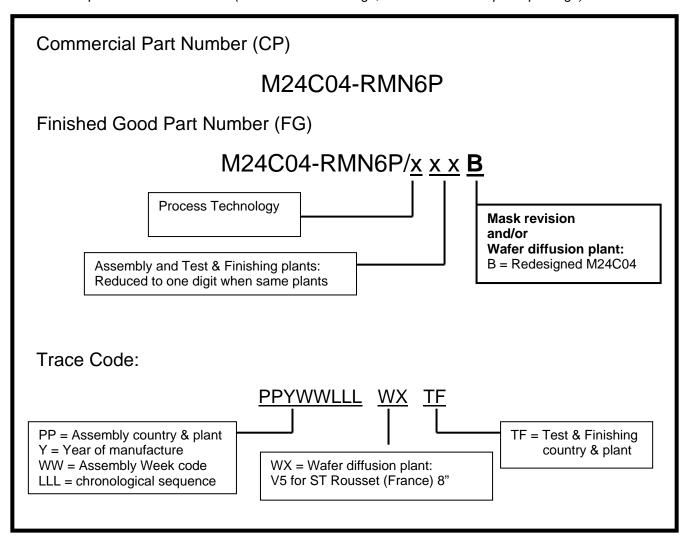
The qualification report QREE0524 will be available by January 2007.

#### How can the change be seen?

#### - BOX LABEL MARKING

On the BOX LABEL MARKING, the change is visible inside the Finished Good Part Number: the **Mask revision and/or Wafer diffusion plant** identifier is "**B**" for the **redesigned version**, the identifier being "A" for the current version.

→ Example for M24C04-RMN6P (1.8V to 5.5V Vcc range, SO8N RoHS\* compliant package)



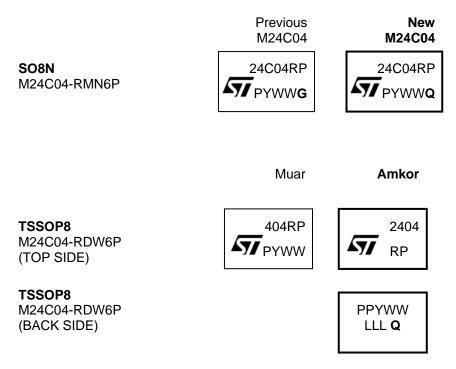
<sup>\*</sup>RoHS: Restriction of the use of certain Hazardous Substances in electrical and electronic equipments

#### How can the change be seen?

#### - DEVICE MARKING

On the DEVICE MARKING of the SO8N package, the change is visible on the top side marking, inside the second line of the trace code (PYWWT): the last digit "T" for the **Process Technology/wafer fab** identifier is "**Q**" for the **redesigned version**, the identifier being "G" for the current version.

On the DEVICE MARKING of TSSOP8 package, the change is visible on the back side of the package, on the first line of the marking, inside the second line of the trace code: the digit for the **Process Technology/wafer fab** identifier is "Q" for the **redesigned version**.



The traceability for each device is as follows:

P (or PP) Y WW T LLL

PP = Assembly country & plant Y = Last digit of the Year of Assembly WW = Assembly Week code T = Process Technology / Wafer Fab LLL = chronological sequence

## **Appendix A- Product Change Information**

Product family / Commercial products:		M24C04 1.8V to 5.5V Vcc range	
Customer(s):		All	
Type of change:		Redesign and die optimization	
Reason for the change:		Production capacity increase and line up to state of the art of low voltage design	
Description of the change:		New design	
Forecast date of the change:		March 2007	
Forecast availability date of qualification sample for the customer(s):		January 2007	
Forecast date for the internal STMicroelectronics change, Qualification report availabilit	y:	January 2007	
Marking to identify the changed product:		Process Technology/Wafer fab identifier is "Q" for the redesigned version	
Description of the qualification program:		Standard ST Microelectronics Corporate Procedures for Quality and Reliability	
Product Line(s) and/or Part Number(s):		M24C04-RMN6P - M24C04-RMN6TP M24C04-RDW6P - M24C04-RDW6TP	
Manufacturing location:		ST AMK (Singapore) 6 inch wafer fab	
Estimated date of first shipment:		March 2007	
Division Product Manager:	C. DARDANNE	Date: December 19, 2006	
Group QA Manager:	F. REDAELLI	Date: January 03, 2007	

### **APPENDIX B: Qualification Plan:**

#### PRODUCT DESCRIPTION

	Device to qualify	Qualified similar device
Product name	M24C04GB	M24C16GA
Memory size	(together with M24C08GB)  4Kb	16Kb

#### **SIMILARITY**

The CMOSF6SPDM 36% Process Technology is already qualified in ST Ang Mo Kio 6 inch wafer fab with the M24C16G (QREE0320) which has a larger or equivalent memory array.

#### **CHARACTERIZATION**

Table 1. Characterization requirements.

Number of lots	Parameters	Vcc range	Temperature range
3	All	1.8V/5.5V	-40°C/85°C

#### **RELIABILITY**

Table 2. Product qualification. Die-related reliability tests

#### **EEPROM**

Abrv.	Test Procedure	Method	Test Conditions	Num of lots	Criteria
EDR	NVM Endurance	AEC-Q100-005	1Mcyc @25C or 100Kcyc @125C cycles, then: - HTSL 150°C, 500hr - HTOL 150°C, 408 hr	1 1	0/77 0/77
ESD HBM	Electrostatic Discharge	AEC-Q100-002	Human Body Model: 1.5kOhms, 100pF 4000V	1	0/9
ESD MM	Electrostatic Discharge	AEC-Q100-003	Machine Model: 0kOhms, 200pF 400V	1	0/9
LU	Latch-up	AEC-Q100-004	Max operating temperature	1	0/6
W/E	Erase/Write cycles and Bake	Internal.	1,000,000 E/W cycles Bake: 150°C, 168hr or 200°C, 48hr	1	0/77

Document Revision History			
Date	Rev.	Description of the Revision	
Dec. 14, 2006	1.00	First draft creation (Christian POLI)	
D		O'contact of O DADDANINE	
Dec. 19, 2006		Signed off C.DARDANNE	
Jan. 03, 2007		Signed off F. REDAELLI	

Source Documents & Reference Documents		
Source document Title	Rev.:	Date:

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