



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-IPC/07/2330
Notification Date 02/23/2007

**2ND SOURCE ASSEMBLY LINE OF PM6685xx device (UN08 line)
& PM6680xx device (UN13 line) - VFQFPN 5X5X1 - IN UTAC THAI SUBCON**

IPC - IND.& POWER CONV.

Table 1. Change Identification

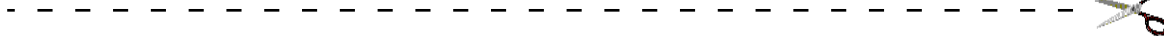
Product Identification (Product Family/Commercial Product)	PM6685, PM6685TR, PM6680 & PM6680TR
Type of change	Package assembly location change
Reason for change	capacity increase
Description of the change	see attachment
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Traceab. assy area code inside marking "FN"
Manufacturing Location(s)	

Table 2. Change Implementation Schedule

Forecasted implementation date for change	16-Feb-2007
Forecasted availability date of samples for customer	15-Mar-2007
Forecasted date for STMicroelectronics change Qualification Plan results availability	16-Feb-2007
Estimated date of changed product first shipment	25-May-2007

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN APM-IPC/07/2330
Please sign and return to STMicroelectronics Sales Office		Notification Date 02/23/2007
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	Name:	
	Title:	
	Company:	
	Date:	
	Signature:	
Remark	

DOCUMENT APPROVAL

Name	Function
Menniti, Pietro	Division Marketing Manager
Borghi, Maria Rosa	Division Product Manager
Motta, Antonino	Division Q.A. Manager



2ND SOURCE ASSEMBLY LINE OF PM6685xx device (UN08 line) & PM6680xx device (UN13 line) - VFQFPN 5X5X1 package - IN UTAC (ex Nseb) Thailand SUBCON

WHAT:

APM-IPC Div. is going to qualify a 2nd source assembly plant in UTAC (ex Nseb) Thailand subcon for the device PM6685xx (UN08 line) & PM6680xx (UN13 line) in VFQFPN 5X5X1 package .

WHY:

Production rationalization and B-end capacity increase

HOW:

according to the attached qualification report

WHEN:

the production will start in Q2, 2007. The relevant samples could be available in March 2007



Q&R Project Code:

RR000407CT6017

QUALITY & RELIABILITY EVALUATION REPORT

New Package Qualification

VQFN32 5X5X1.0

***UN13ABH-BCD5s**

VQFN24 4X4X1.0

***UN19 AA1 - BCD5s**

PB FREE solution (Sn 100%)

UTAC (EX NSEB) THAILAND SUBCONTRACTOR

Abstract:

A qualification exercise it was done, to qualify the new **VQFN32 5X5X1.0 / VQFN24 4X4X1.0** using as test vehicles ***UN13ABH** and ***UN19AA1** on UTAC subcontractor manufacturing assy plant.

Conclusion:

On the basis of the already achieved positive results; IQC/ Workability & testing reports, Reliability evaluation/Construction Analysis for both PKG/lines we can issued a full qualification for all the I&PC involved lines assembled in **VQFN32 5X5X1.0 / VQFN24 4X4X1.0 UTAC subcontractor manufacturing.**

Note:

Products pass JEDEC LEV.@3 260°C

Issued by
Francesco Ventura
(I&PC QA&R B-END)

Approved by
Antonino Motta
(I&PC /QA&R MNG)



Reliability test conditions and results for *UN13ABH-BCD5s

Test	Test short description					
	Performed on 3# STD assy lots					
	Method	Conditions	Sample /Lots	Number of lots	Duration	Results Fail/SS
PC	Pre-Conditioning: Moisture sensitivity level 3					
	SAM T=0 & AFTER PRECOND	192h 30°C/60% - 3 reflow PBT 260°C	100	#3		0/300 NO-DELAMINATION
E.S :	Preconditioning JL@3 + Pressure pot					
	Conditions:	2atm	50	#3	168hrs	0/150
E.S :	Preconditioning JL@3 + Thermal Cycle					
	Conditions:	Ta=-50°C/+150°C	50	#3	1000Cy	0/150
HTS	High Temperature Storage					
	No bias	Tamb=150°C	50	#3	1000h	0/150
E.S.:	High Temperature Storage+ Thermal Cycle					
		HTS:no bias, Ta=150°C, T.C.>500Cy, air	100	#1	500h	0/100
H.T.R.B	High Temperature Reverse Bias	Tj=150°C;500hrs Vin=38V, vcc=6V, Vboot=44V	28	#3	500h	0/84
ESD	Electro Static Discharge					
	Charge Device Model	+/- 1KV	5			0/5



Device construction note *UN13ABH-BCD5s

DIE FEATURES	
Die Code	: PUN13ABH
Diffusion process	: A1 BCD5/BCD5S REV.D
Wafer diameter	: 6"
Diffusion site	: CARROLLTON
Die size	: 2310 X 2310UM
Die Tick.	: 280 ± 20 µm
Passivation	: USG-PSG +SION-PIX
Back finishing	: CHROMIUM/NICKEL/GOLD

PACKAGE FEATURES	
Technical code(PKG)	: 42
Package name	: VFQFPN32L 5X5 X1.0
Assembly site	: UTAC THAILAND
Leadframe / substrate	: VFQFPN32L 5X5 2 ring Ag plating
Die attach	: GLUE ABLEBOND 8600
Wire Bonding	: 1.0 mils Au
Solder balls / plating	: Sn100% (Pure Tin)
Assy lot	: NA

Attachments:

- Reliability tests description (MANDATORY)
- MBD(Mont & Bond Diagram) for both line/pkg



Reliability test conditions and results for *UN19ABH-BCD5s

Test	Test short description					
	Performed on 3# STD assy lots					
	Method	Conditions	Sample /Lots	Number of lots	Duration	Results Fail/SS
PC	Pre-Conditioning: Moisture sensitivity level 3					
	SAM T=0 & AFTER PRECOND	192h 30°C/60% - 3 reflow PBT 260°C	100	#1		0/100 NO DELAMINATION
E.S :	Preconditioning JL@3 + Pressure pot					
	Conditioning:	2atm	50	#1	168hrs	0/50
E.S :	Preconditioning JL@3 + Thermal Cycle					
	Conditions:Ta=-50°C/+150°C		50	#1	1000Cy	0/50
HTS	High Temperature Storage					
	No bias	Tamb=150°C	50	#1	1000h	0/50
ESD	Electro Static Discharge					
	Charge Device Model	+/- 1.5KV	5			0/5



Device construction note *UN19AA1-BCD5s

DIE FEATURES	
Die Code	: SUN19AA1
Diffusion process	: 20 BCD5C/BCD5S CLEAN PROCESS 8
Wafer diameter	: 6"
Diffusion site	: CARROLLTON
Die size	: 1900 X 1900UM
Die Tick.	: 280 ± 20 µm
Passivation	: TEOS+PTEOS+SiOn+PIX

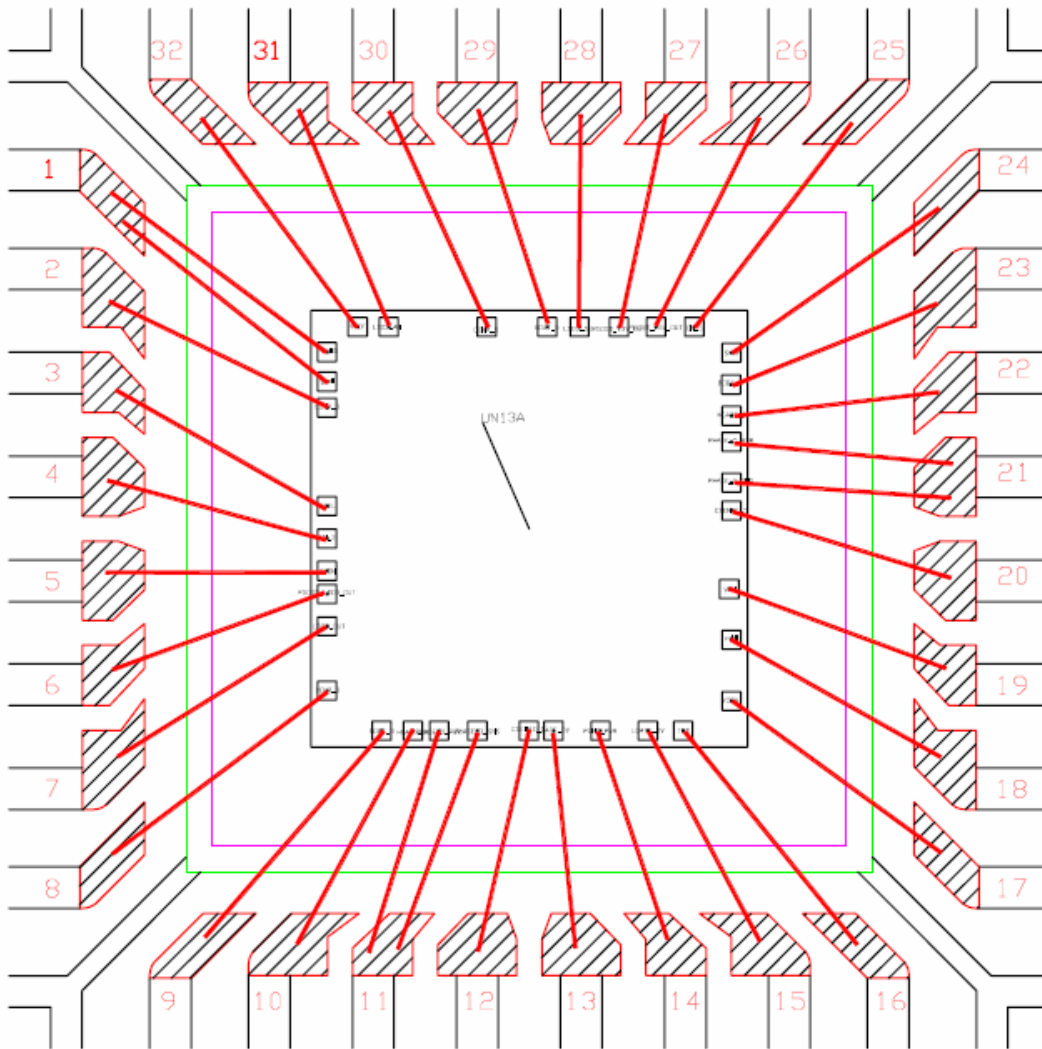
PACKAGE FEATURES	
Technical code(PKG)	: ND
Package name	: VFQFPN24L 4X4 X1.0
Assembly site	: UTAC THAILAND
Leadframe / substrate	: VFQFPN24L 4X4 Ag plating
Die attach	: GLUE ABLEBOND 8200T
Wire Bonding	: 1.0 mils Au
Solder balls / plating	: Sn100% (Pure Tin)



TITLE: MOUNT BOND DIAGRAM FOR F542*UN13ABH AMKOR

FRAME PAD: $\frac{130 \times 130 \text{ mils}}{3,300 \times 3,300 \text{ mm}}$

MAX DIE SIZE: $\frac{120 \times 120 \text{ mils}}{3,046 \times 3,046 \text{ mm}}$



Scale : $\frac{1 \text{ mm}}$

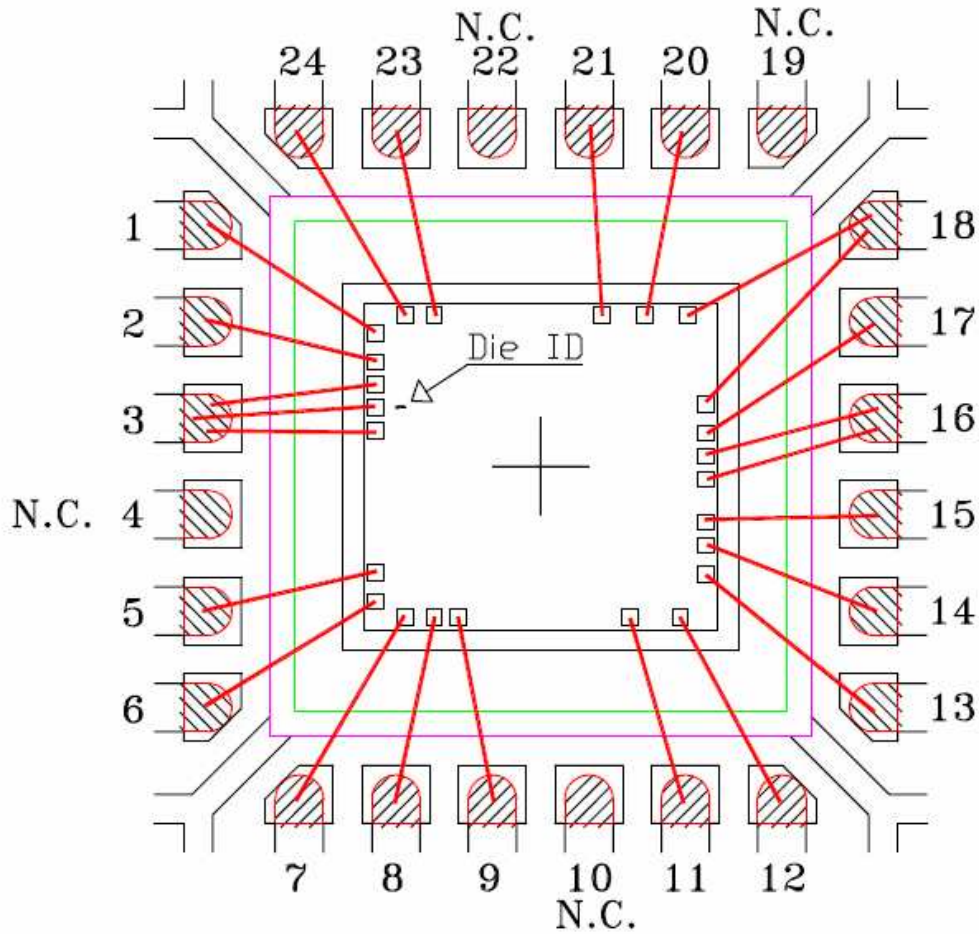
NOTE: E.S.D. PROGRAM IS MANDATORY



TITLE: MOUNT AND BOND DIAGRAM FOR A5ND*UN19AA1 NSE

FRAME PAD : $\frac{110,24 \times 110,24 \text{ mils}}{2,800 \times 2,800 \text{ mm}}$

MAX DIE SIZE : $\frac{100,24 \times 100,24 \text{ mils}}{2,546 \times 2,546 \text{ mm}}$



Scale : $\frac{1 \text{ mm}}{\text{---}}$

E.S.D. PROGRAM IS MANDATORY



ATTACHMENT 1: RELIABILITY TEST DESCRIPTION

TEST NAME	DESCRIPTION	PURPOSE
JLn: Jedec Level n surface mounting simulation	The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.	As stand-alone test: to investigate the level of moisture sensitivity. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
TCT: Temperature Cycles Test	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation.
PPT: Pressure Pot Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
HTS: High Temperature Storage	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
TST: Thermal Shock Test	The device is submitted to cycled thermal shocks through alternate immersion in a hot and a cold oil bath.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation.
HTRB: High Temperature Reverse Bias Test	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: -) low power dissipation; -) max. supply voltage compatible with diffusion process and internal circuitry limitations; -) max. junction temperature.	To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
THB: Temperature Humidity Bias Test	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To investigate failure mechanisms activated in the die-package environment by electrical field and wet conditions. Typical failure mechanisms are electro-chemical corrosion and surface effects related to the moulding compound.



<p>E.S.D</p>	<p>This test is performed to verify adequate pin protection to electrostatic discharges. The flow chart is the following:</p> <ul style="list-style-type: none">▪<ul style="list-style-type: none">• Initial testing @ Ta=25°C• ESD discharging @ Ta=25°C• Final Testing @ Ta=25°C	<p>TEST CONDITIONS:</p> <ul style="list-style-type: none">○ Charge Device Model JEDEC STANDARD JESD22-C101-A
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