



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-SNV/07/2498
Notification Date 05/03/2007

M95512, 512Kbit Serial SPI Bus EEPROM

SNV - MEMORY

Table 1. Change Identification

Product Identification (Product Family/Commercial Product)	M95512 products family
Type of change	Product design change
Reason for change	Production capacity increase and line up to state of art of design
Description of the change	New design
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Process Techno ID is "B" on SO8 package
Manufacturing Location(s)	

Table 2. Change Implementation Schedule

Forecasted implementation date for change	01-Aug-2007
Forecasted availability date of samples for customer	01-Jul-2007
Forecasted date for STMicroelectronics change Qualification Plan results availability	01-Jul-2007
Estimated date of changed product first shipment	01-Aug-2007

DOCUMENT APPROVAL

Name	Function
Poli, Christian	Division Marketing Manager
Rodrigues, Benoit	Division Product Manager
Yackowlew, Nicolas	Division Q.A. Manager



**M95512, 512Kbit Serial SPI Bus EEPROM
Redesign and Die Optimization**

What is the change?

The M95512, 512Kbit Serial SPI Bus EEPROM product family, produced in the CMOSF8L Process Technology, will be redesigned and optimized using the same Process Technology in the same Wafer diffusion plant.

Why?

The strategy of STMicroelectronics Memory Division is to support the growth of our customers on a long-term basis. In line with this commitment, the qualification of the redesigned M95512 die in the same CMOSF8L Process Technology will increase the production capacity throughput, reduce the lead-time and consequently improve the service to our customers.

When?

The production of the new M95512 in the ST Rousset (France) 8 inch wafer diffusion plant will ramp up from June 2007 and shipments will start from August 2007 onward. The phase out of the current version will start from August 2007 with a completion planned for October 2007.

How will the change be qualified?

The new version of the M95512 will be qualified using the standard ST Microelectronics Corporate Procedures for Quality and Reliability. The qualification report QREE0703 will be available in July 2007.

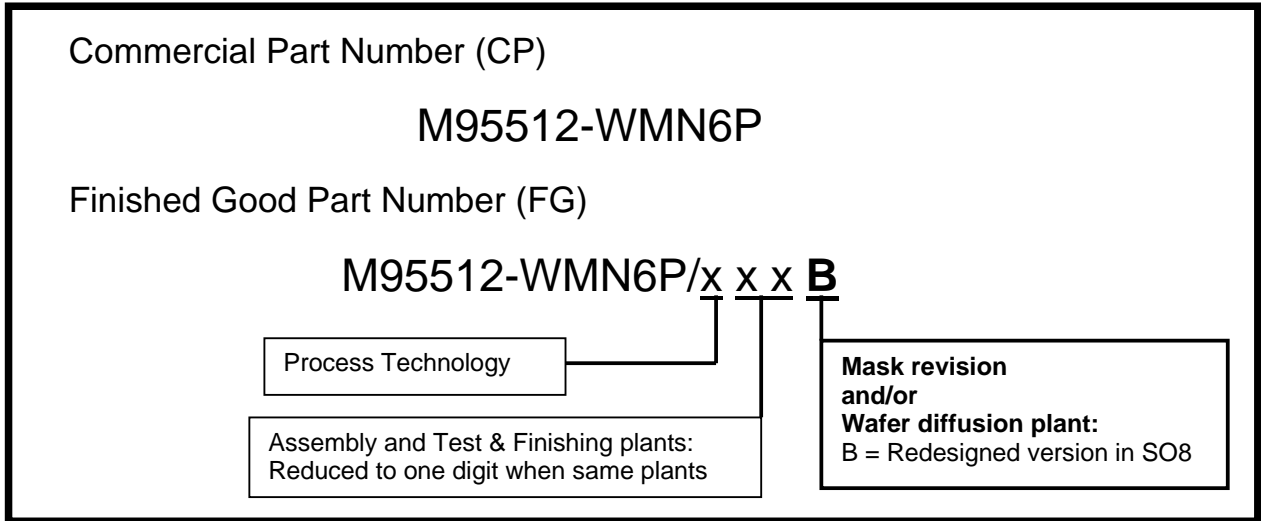
How can the change be seen?

- BOX LABEL MARKING

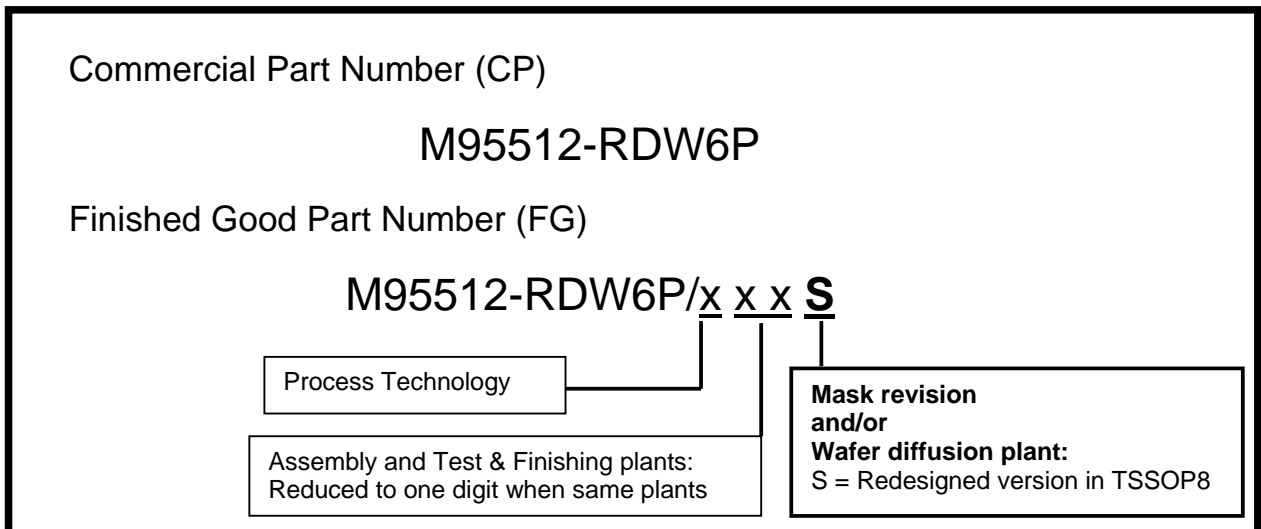
On the BOX LABEL MARKING, the change is visible inside the Finished Good Part Number: the **Mask revision and /or Wafer diffusion plant** identifier is:

- **“B”** for the **redesigned version in SO8N**
- **“S”** for the **redesigned version in TSSOP8**

→ Example for M95512-WMN6P (2.5V to 5.5V Vcc range, SO8N RoHS* compliant package)



→ Example for M95512-RDW6P (1.8V to 5.5V Vcc range, TSSOP8 RoHS* compliant package)



*RoHS: Restriction of the use of certain Hazardous Substances in electrical and electronic equipments

How can the change be seen?

- DEVICE MARKING

On the DEVICE MARKING of the SO8N package, the change is visible on the top side marking, inside the second line of the trace code (PYWWT): the last digit “T” for **Process Technology** identifier is “B” for the **redesigned version**, the identifier being “A” for the previous version.



The traceability for each device is as follows:

P Y WW T

<p>P = Assembly country & plant Y = Last digit of the Year of Assembly WW = Assembly Week code T = Process Technology code/ Wafer Fab ID</p>

For the TSSOP8 package, the change is only visible on the BOX LABEL MARKING (see previous page).

Appendix A- Product Change Information

Product family / Commercial products:	M95512 products family
Customer(s):	All
Type of change:	Redesign and die optimization
Reason for the change:	Production capacity increase and line up to state of art of design
Description of the change:	New design
Forecast date of the change:	August 2007
Forecast availability date of qualification sample for the customer(s):	July 2007
Forecast date for the internal STMicroelectronics change, Qualification report availability:	July 2007
Marking to identify the changed product:	Process and fab ID see marking above
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See list of concerned products in appendix B
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	August 2007
Division Product Manager: B. RODRIGUES	Date:
Group QA Manager: N. YACKOWLEW	Date:

Appendix B: concerned products:

M95512-WMN6P
M95512-WMN6TP
M95512-WDW6TP
M95512-RMN6P
M95512-RMN6TP
M95512-RDW6TP
M95512-RAW21/90 (*)

(*) Please contact ST sales office for equivalent bare die product.

Appendix C: Qualification Plan:

PRODUCT DESCRIPTION

	Device to qualify
Product name	M95512 / M24512 New Design
Memory size	512K

SIMILARITY

CMOSF8L technology already qualified in R8" Fab. 512Kb already qualified using F8L technology.

CHARACTERIZATION

Table 1. Characterization requirements.

RELIABILITY

Table 2. Product qualification. Die-related reliability tests

Number of lots	Parameters	Vcc range	Temperature range
3	All	1.8V/5.5V	-40°C/125°C

EEPROM

Abv.	Test Procedure	Method	Test Conditions	Num of lots	Criteria
EDR	NVM Endurance	AEC-Q100-005	1Mcyc @25C or 100Kcyc @125C cycles, then: - HTSL 150°C, 1000 hrs - HTOL 150°C, 1000 hrs	1 1	0/80 0/80
HTB	High Temperature Bake	Internal	200°C, 1000 hrs	1	0/80
LTOL	Low Temperature Operating Life	Mil Std 883 Method 1005	-40°C, VCC+20%, 1000 hrs	1	0/80
W/E	Erase/Write cycles and Bake	Internal.	Up to 10M E/W cycles Bake: 200°C, 48hr	1	0/80
ESD HBM	Electrostatic Discharge	AEC-Q100-002	Human Body Model: 1.5k , 100pF : Up to 4500V (step 500V)	1	0/81
ESD MM	Electrostatic Discharge	AEC-Q100-003	Machine Model: 0k , 200pF, 250V & 400V	1	0/18
LU	Latch-up	AEC-Q100-004	Class II Level A (Max operating temperature)	1	0/6

Table 2. Product qualification. Package-related reliability tests (SO8N Shenzhen / SO8N Amkor / TSSOP8 Amkor / SO8W ChipPac)

Test Procedure	Method	Test Conditions	Num of lots	Criteria
Electrostatic Discharge CDM	AEC-Q100-011	Charge Device Model (Field Induced CDM) : Up to 1500V (step 250V)	1	0/18

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