



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/09/4475
Notification Date 04/13/2009

**M95512, 512Kbit Serial SPI Bus EEPROM Redesign and
Upgrade to the CMOSF8H Process Technology**

Table 1. Change Implementation Schedule

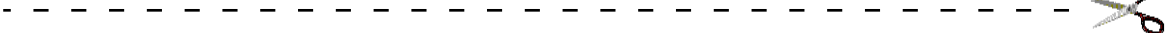
| | |
|--|-------------|
| Forecasted implementation date for change | 06-Apr-2009 |
| Forecasted availability date of samples for customer | 06-Apr-2009 |
| Forecasted date for STMicroelectronics change Qualification Plan results availability | 06-Apr-2009 |
| Estimated date of changed product first shipment | 13-Jul-2009 |

Table 2. Change Identification

| | |
|---|---|
| Product Identification (Product Family/Commercial Product) | M95512 products family |
| Type of change | Waferfab process change |
| Reason for change | Line up to state of art of design |
| Description of the change | Redesign and Upgrade to the new CMOSF8H Process Technology. |
| Product Line(s) and/or Part Number(s) | See attached |
| Description of the Qualification Plan | See attached |
| Change Product Identification | "K" for the new F8H version |
| Manufacturing Location(s) | |

Table 3. List of Attachments

| | |
|----------------------------|--|
| Customer Part numbers list | |
| Qualification Plan results | |



| | | |
|--|------------|------------------------------|
| Customer Acknowledgement of Receipt | | PCN MMS-MMY/09/4475 |
| Please sign and return to STMicroelectronics Sales Office | | Notification Date 04/13/2009 |
| <input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved | Name: | |
| | Title: | |
| | Company: | |
| | Date: | |
| | Signature: | |
| Remark | | |

DOCUMENT APPROVAL

| Name | Function |
|----------------------|----------------------------|
| Leduc, Hubert | Division Marketing Manager |
| Rodrigues, Benoit | Division Product Manager |
| Malbranche, Jean-Luc | Division Q.A. Manager |



**M95512, 512Kbit Serial SPI Bus EEPROM
Redesign and Upgrade to the CMOSF8H Process Technology**

What is the change?

The **M95512**, 512Kbit Serial SPI Bus EEPROM product family, currently produced using the CMOSF8L Process Technology in the ST Rousset (France) 8 inch wafer diffusion plant has been redesigned and will be upgraded to the new **CMOSF8H** Process Technology in the same wafer diffusion plant.

- AC product performance is improved (20MHz at Vcc=5V, 10MHz at Vcc=2.5V, 5MHz at Vcc=1.8V)
- ESD HBM passes 3000V

Upgraded version is functionally backward compatible to previous version, as per datasheet rev.9 dated July 2008.

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M95512 in the new CMOSF8H Process Technology will increase the production capacity throughput and consequently improve the service to our customers.

Also, the new die is fitting inside the MLP 2x3 package (M95512-RMB6TG).

When?

The production of the upgraded M95512 with the new CMOSF8H will ramp up from middle of April 2009 and shipments can start from middle of July 2009 onward (upon customer approval).

How will the change be qualified?

The new version of the M95512 will be qualified using the standard ST Microelectronics Corporate Procedures for Quality and Reliability.

The **Qualification Report QREE0807** will be available Week 18.

What is the impact of the change?

- **Form:** marking change (see **Device marking** paragraph)
- **Fit:** no change
- **Function:** change on **AC performances** and **ESD HBM**

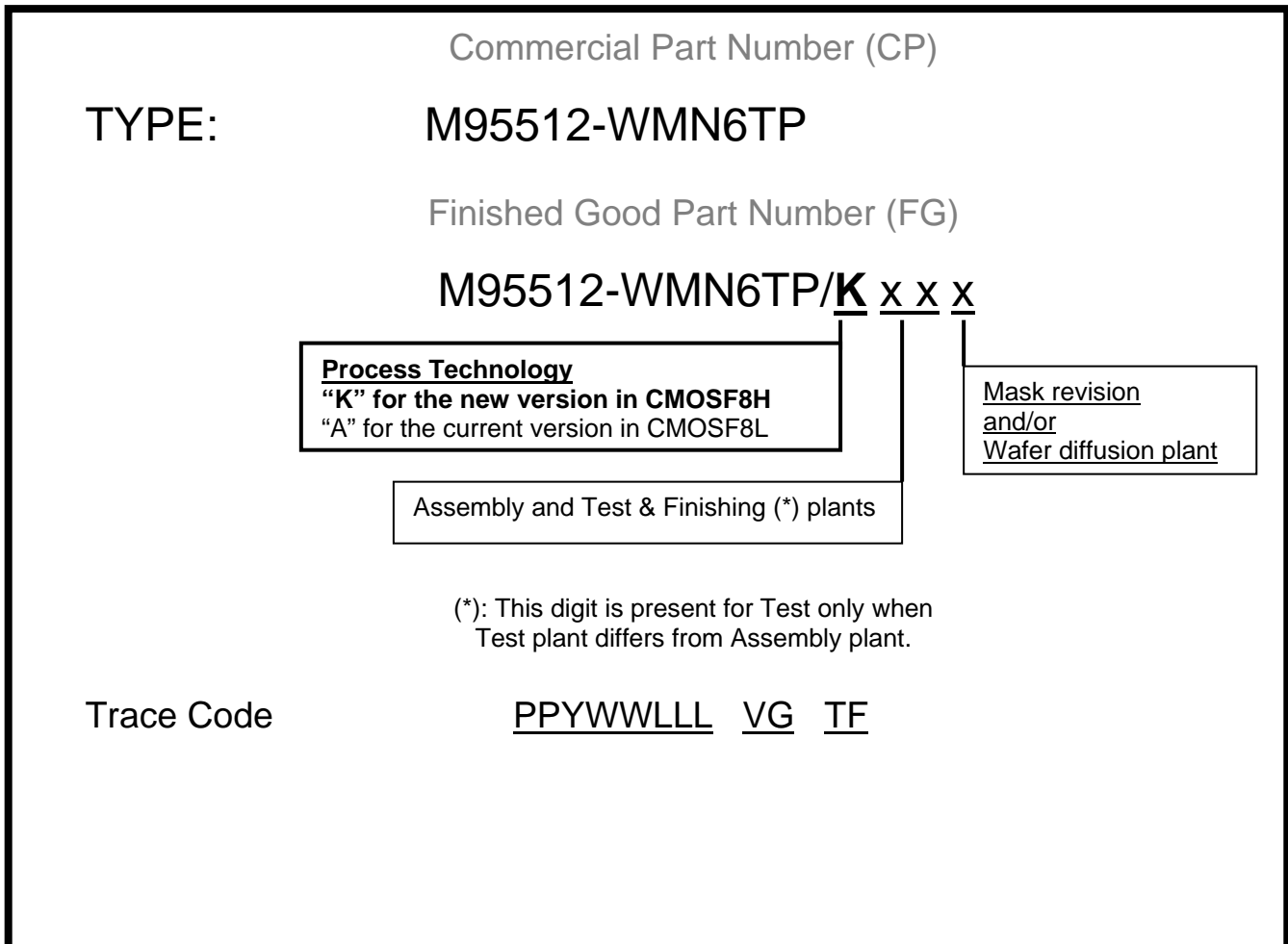
How can the change be seen?

- **BOX LABEL MARKING**

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **Process Technology** identifier is “K” for the **upgraded version**, this identifier being “A” for the current version.

→ *Example for M95512-WMN6TP (2.5V to 5.5V Vcc range, SO8N RoHS* compliant package)*

*RoHS: Restriction of the use of certain Hazardous Substances in electrical and electronic equipments



How can the change be seen?

- DEVICE MARKING

On the DEVICE MARKING of the **SO8N** package, the difference is visible inside the trace code (PYWWT) where the last digit “T” for **Process Technology** identifier is “K” for the **upgraded version** in **CMOSF8H**, the identifier being “B” for the current version in CMOSF8L.



| | | |
|--|---|--|
| | Upgraded M95512 in CMOSF8H | Current M95512 in CMOSF8L |
| SO8N Example: M95512-WMN6TP |  |  |

The traceability for each device is as follows:

P Y W W T

| |
|---|
| P = Assembly plant Y = Last digit of the Year of Assembly WW = Assembly Week code T = Process Technology code/ Wafer Fab ID |
|---|

For **TSSOP8**, the difference is visible inside the product name: **upgraded version** in **CMOSF8H** is ending by “K”, the current version was ending by “P”.

| | | |
|--|---|--|
| | Upgraded M95512 in CMOSF8H | Current M95512 in CMOSF8L |
| TSSOP8 Example: M95512-WDW6TP |  |  |

The traceability for each device is as follows:

P Y W W

| |
|---|
| P = Assembly plant Y = Last digit of the Year of Assembly WW = Assembly Week code |
|---|

Appendix A- Product Change Information

| | |
|--|--|
| Product family / Commercial products: | M95512 products family |
| Customer(s): | All |
| Type of change: | Wafer fab Process Technology change |
| Reason for the change: | Line up to state of art of design. |
| Description of the change: | Redesign and Upgrade to the new CMOSF8H Process Technology. |
| Forecast date of the change: | Week 15 / 2009 |
| Forecast date of <u>Qualification samples</u> availability for customer(s): | M95512-WDW6TP → Available M95512-WMN6TP → Available M95512-RMN6TP → Week 18 M95512-RDW6TP → Week 19 |
| Forecast date for the internal STMicroelectronics change, <u>Qualification Report</u> availability: | Week 18 / 2009 |
| Marking to identify the changed product: | Process and fab ID see marking above |
| Description of the qualification program: | Standard ST Microelectronics Corporate Procedures for Quality and Reliability |
| Product Line(s) and/or Part Number(s): | M95512-RDW6TP M95512-RMN6TP M95512-WDW6TP M95512-WMN6TP |
| Manufacturing location: | Rousset 8 inch wafer fab |
| Estimated date of first shipment: | Week 29 / 2009 |

Appendix B: Intermediate Qualification Report:



QREE0807

Intermediate qualification report

New design / M95512
 using the CMOSF8H technology in the Rousset 8" Fab

Table 1. Product information

| General information | |
|---|---|
| Commercial product | M95512-RMN6TP M95512-WMN6TP M95512-RDW6TP M95512-WDW6TP M95512-RMB6TG |
| Product description | 512 Kbit serial SPI bus EEPROM with high-speed clock |
| Product group | MMS |
| Product division | MMY - Memory |
| Silicon process technology | CMOSF8H |
| Wafer fabrication location | RS8F - ST Rousset 8", France |
| Electrical Wafer Sort test plant location | ST Rousset, France |

Table 2. Package description

| Package description | Assembly plant location | Final test plant location |
|----------------------------|-------------------------|---------------------------|
| SO8N | ST Shenzhen, China | ST Shenzhen, China |
| | Amkor P1, Philippines | Amkor P3, Philippines |
| TSSOP8 | ST Shenzhen, China | ST Shenzhen, China |
| | Amkor P1, Philippines | Amkor P3, Philippines |
| UFDFPN8 (MLP8) 2 x 3 mm | Amkor P3, Philippines | Amkor P3, Philippines |

Reliability / Qualification assessment: 504 hrs PASS on 2 lots - Pending reliability results 1008 hrs

Note: This document will remain a draft until the product is qualified.

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new design M95512 using the CMOSF8H silicon process technology in the ST Rousset 8" diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at -40 to 85 °C for M95512-W devices
- 1.8 to 5.5 V at -40 to 85 °C for M95512-R devices

The CMOSF8H is a new advanced silicon process technology in the ST Rousset 8" fab, with Double Poly and Double Metal process. This document serves for the qualification of the named product and the named silicon process technology in the named diffusion fab.

1.2 Conclusion

The new design M95512 using the CMOSF8H silicon process technology in the ST Rousset 8" diffusion fab has passed all ESD and latch-up requirements. Product validation and reliability trials are ongoing.

Refer to [Section 3: Reliability test results](#) for details.

2 Device characteristics

Device description

This electrically erasable programmable memory (EEPROM) device is accessed by a high-speed SPI-compatible bus. The memory array is organized as 65536 x 8 bits.

The device is accessed by a simple serial interface that is SPI-compatible. The bus signals are C, D and Q.

The device is selected when Chip Select (\overline{CS}) is taken low. Communications with the device can be interrupted using Hold (HOLD).

Refer to the product datasheet for more details.

DRAFT

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in [Table 3](#).

Table 3. Product vehicles used for die qualification

| Product | Silicon process technology | Wafer fabrication location | Package description | Assembly plant location |
|---------|----------------------------|----------------------------|---------------------|--------------------------|
| M95512 | CMOSF8H | ST Rousset 8* | CDIP8 | Engi assy ⁽¹⁾ |

1. CDIP8 is a ceramic package used only for die-oriented reliability trials.

The product vehicle and silicon process technologies used for package qualification are presented in [Table 4](#).

Table 4. Product vehicles used for package qualification

| Product | Silicon process technology | Wafer fabrication location | Package description | Assembly plant location |
|----------------------------|----------------------------|----------------------------|---------------------|-------------------------|
| M95512 | CMOSF8H | ST Rousset 8* | SO8N | ST Shenzhen |
| | | | | Amkor P1 |
| | | | TSSOP8 | ST Shenzhen |
| | | | | Amkor P1 |
| UFDFPN8 (MLP8) 2 x 3 mm | Amkor P3 | | | |

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in [Table 5](#) for die-oriented tests
- in [Table 6](#) for TSSOP8 Shenzhen package-oriented tests
- Reliability tests on all other packages are planned, but results are not yet available.

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Reliability test results

Table 5. Die-oriented reliability test plan and result summary (CDIPs / Engineering package)⁽¹⁾

| Test | Test short description | | | | | | | |
|-------------------------------|---|--|--------------------|-------------|---------------------------|----------------------------|------------------|----------------|
| | Method | Conditions | Sample size / lots | No. of lots | Duration | Results fail / sample size | | |
| | | | | | | M95512 | | |
| | | | | | | Lot 1 | Lot 2 | Lot 3 |
| EDR | High temperature operating life after endurance | | | | | | | |
| | AEC-Q100-005 | 1 Million E/W cycles at 25 °C then: HTOL 150 °C, 6 V | 80 | 3 | 504 hrs | 0/80 | 0/80 | Results W17'09 |
| | | | | | 1008 hrs | Results W15'09 | Results W15'09 | Results W21'09 |
| | Data retention after endurance | | | | | | | |
| AEC-Q100-005 | 1 Million E/W cycles at 25 °C then: HTSL at 150 °C | 80 | 3 | 504 hrs | 0/80 | 0/80 | Results W17'09 | |
| | | | | 1008 hrs | Results W15'09 | Results W15'09 | Results W21'09 | |
| LTOL | Low temperature operating life | | | | | | | |
| | JESD22-A108 | -40 °C, 6 V | 80 | 3 | 504 hrs | 0/80 | 0/80 | Results W17'09 |
| | | | | | 1008 hrs | Results W15'09 | Results W15'09 | Results W21'09 |
| High temperature storage life | | | | | | | | |
| HTSL | AEC-Q100-005 JESD22-A103 | Retention bake at 200 °C | 80 | 3 | 504 hrs | 0/80 | 0/80 | Results W17'09 |
| | | | | | 1008 hrs | Results W15'09 | Results W15'09 | Results W21'09 |
| WEB | Program/erase endurance cycling + bake | | | | | | | |
| | Internal spec. | 1 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours | 80 | 3 | 1 Million cycles / 48 hrs | 0/80 | 0/80 | 0/80 |
| ESD HBM | Electrostatic discharge (human body model) | | | | | | | |
| | AEC-Q100-002 JESD22-A114 | C = 100 pF, R = 1500 Ω | 27 | 3 | N/A | Pass > 3000 V | Pass > 3000 V | Pass > 3000 V |
| ESD MM | Electrostatic discharge (machine model) | | | | | | | |
| | AEC-Q100-003 JESD22-A115 | C = 200 pF, R = 0 Ω | 6 | 3 | N/A | Pass > 300 V | Pass > 300 V | Results W15'09 |
| LU | Latch-up (current injection and overvoltage stress) | | | | | | | |
| | AEC-Q100-004 JESD78A | At maximum operating temperature (150 °C) | 6 | 3 | N/A | Class II Level A | Class II Level A | Results W15'09 |

1. See [Table 7. List of terms](#) for a definition of abbreviations.



**M95512, 512Kbit Serial SPI Bus EEPROM
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Reliability test results

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Table 6. Package-oriented reliability test plan and result summary (TSSOP8 / Shenzhen) ⁽¹⁾

| Test | Test short description | | | | | | | |
|---------------------|---|---|--------------------|-------------|-------------|----------------------------|----------------|----------------|
| | Method | Conditions | Sample size / lots | No. of lots | Duration | Results fail / sample size | | |
| | | | | | | M95512 | | |
| | | | | | | Lot1 | Lot2 | Lot3 |
| PC | Preconditioning: moisture sensitivity level 1 | | | | | | | |
| | JESD22-A113 J-STD-020D | MSL1, peak temperature at 260 °C, 3 IReflow | 345 | 3 | N/A | 0/345 | 0/345 | 0/345 |
| THB ⁽²⁾ | Temperature humidity bias | | | | | | | |
| | AEC-Q100- JESD22-A101 | 85 °C, 85% RH, bias 5.5 V | 80 | 3 | 1008 hrs | 0/80 | 0/80 | 0/80 |
| TC ⁽²⁾ | Temperature cycling | | | | | | | |
| | AEC-Q100- JESD22-A104 | -65 °C / +150 °C | 80 | 3 | 1000 cycles | 0/80 | 0/80 | 0/80 |
| TMSK ⁽²⁾ | Thermal shocks | | | | | | | |
| | JESD22-A106 | -55 °C / +125 °C | 25 | 3 | 200 shocks | 0/80 | 0/80 | 0/80 |
| AC ⁽²⁾ | Autoclave (pressure pot) | | | | | | | |
| | AEC-Q100- JESD22-A102 | 121 °C, 100% RH at 2 ATM | 80 | 3 | 168 hrs | 0/80 | 0/80 | 0/80 |
| HTSL ⁽²⁾ | High temperature storage life | | | | | | | |
| | AEC-Q100- JESD22-A103 | Retention bake at 150 °C | 80 | 3 | 1008 hrs | 0/80 | 0/80 | 0/80 |
| ELFR | Early life failure rate | | | | | | | |
| | AEC-Q100- 008 | HTOL 150 °C, 6 V | 800 | 3 | 48 hrs | Results W24'09 | Results W24'09 | Results W24'09 |
| ESD CDM | Electrostatic discharge (charge device model) | | | | | | | |
| | AEC-Q100- JESD22-C101 | Field induced charging method | 18 | 1 | N/A | Pass >1500 V | - | - |

1. See [Table 7. List of terms](#) for a definition of abbreviations.

2. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78A: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 7. List of terms

| Terms | Description |
|---------|--|
| EDR | NVM endurance, data retention and operational life |
| HTOL | High temperature operating life |
| LTOL | Low temperature operating life |
| HTB | High temperature bake |
| WEB | Program/Erase endurance cycling + bake |
| ESD HBM | Electrostatic discharge (human body model) |
| ESD MM | Electrostatic discharge (machine model) |
| LU | Latch-up |
| PC | Preconditioning (solder simulation) |
| THB | Temperature humidity bias |
| TC | Temperature cycling |
| TMSK | Thermal shocks |
| AC | Autoclave (pressure pot) |
| HTSL | High temperature storage life |
| ELFR | Early life failure rate |
| ESD CDM | Electrostatic discharge (charge device model) |

| Document Revision History | | |
|----------------------------------|-------------|------------------------------------|
| Date | Rev. | Description of the Revision |
| Apr. 06, 2009 | 1.00 | First draft creation |
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| Source Documents & Reference Documents | | |
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