PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/10/5840
Notification Date 08/20/2010

GLOBALFOUNDRIES FAB2, additional wafer diffusion plant
for the M24C02-R & M24C01-R devices

Table 1. Change Implementation Schedule

Forecasted implementation date for change	13-Aug-2010
Forecasted availabillity date of samples for customer	13-Aug-2010
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	13-Aug-2010
Estimated date of changed product first shipment	19-Nov-2010

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M24C02-R & M24C01-R
Type of change	Waferfab additional location
Reason for change	Wafer fab second source
Description of the change	GLOBALFOUNDRIES FAB2, additional wafer fab for M24C02-R & M24C01-R devices
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Process Technology identifier "T" is "$" for Globalfoundries version
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

Customer Acknowledgement of Receipt	**PCN MMS-MMY/10/5840**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 08/20/2010**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Leduc, Hubert	Division Marketing Manager
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Malbranche, Jean-Luc	Division Q.A. Manager

PRODUCT / PROCESS CHANGE NOTIFICATION

GLOBALFOUNDRIES FAB2, additional wafer diffusion plant for the M24C02-R & M24C01-R devices

What is the change?

The **M24C02-R & M24C01-R**, 2Kbit & 1Kbit Serial I²C Bus EEPROM, currently produced at ST Ang Mo Kio (Singapore) 6 inch wafer diffusion plant using the CMOSF6SP36% DM process technology will be now also produced in the **GLOBALFOUNDRIES (Singapore) subcontractor 8 inch wafer diffusion plant** using the same process technology.

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M24C02-R & M24C01-R devices at GLOBALFOUNDRIES (Singapore) wafer diffusion plant will secure a second source after ST Ang Mo Kio (Singapore) and allow for a further increase of the production throughput and consequently improve the service to our customers.

When?

The production of the M24C02-R & M24C01-R devices at GLOBALFOUNDRIES (Singapore) 8 inch wafer diffusion plant will ramp up from September 2010 and shipments can start from middle of November 2010 onward.

How will the change be qualified?

The qualification of the M24C02-R & M24C01-R at GLOBALFOUNDRIES (Singapore) was performed following the standard ST Microelectronics Corporate Procedures for Quality and Reliability.
The CMOSF6SP36% process technology is already qualified and running in large volume in GLOBALFOUNDRIES on many other products.

The **Qualification Report QREE0825** is available and included inside this document.

What is the impact of the change?

- **Form:** marking change (see **Device marking** paragraph)
- **Fit:** no change
- **Function:** no change

How can the change be seen?

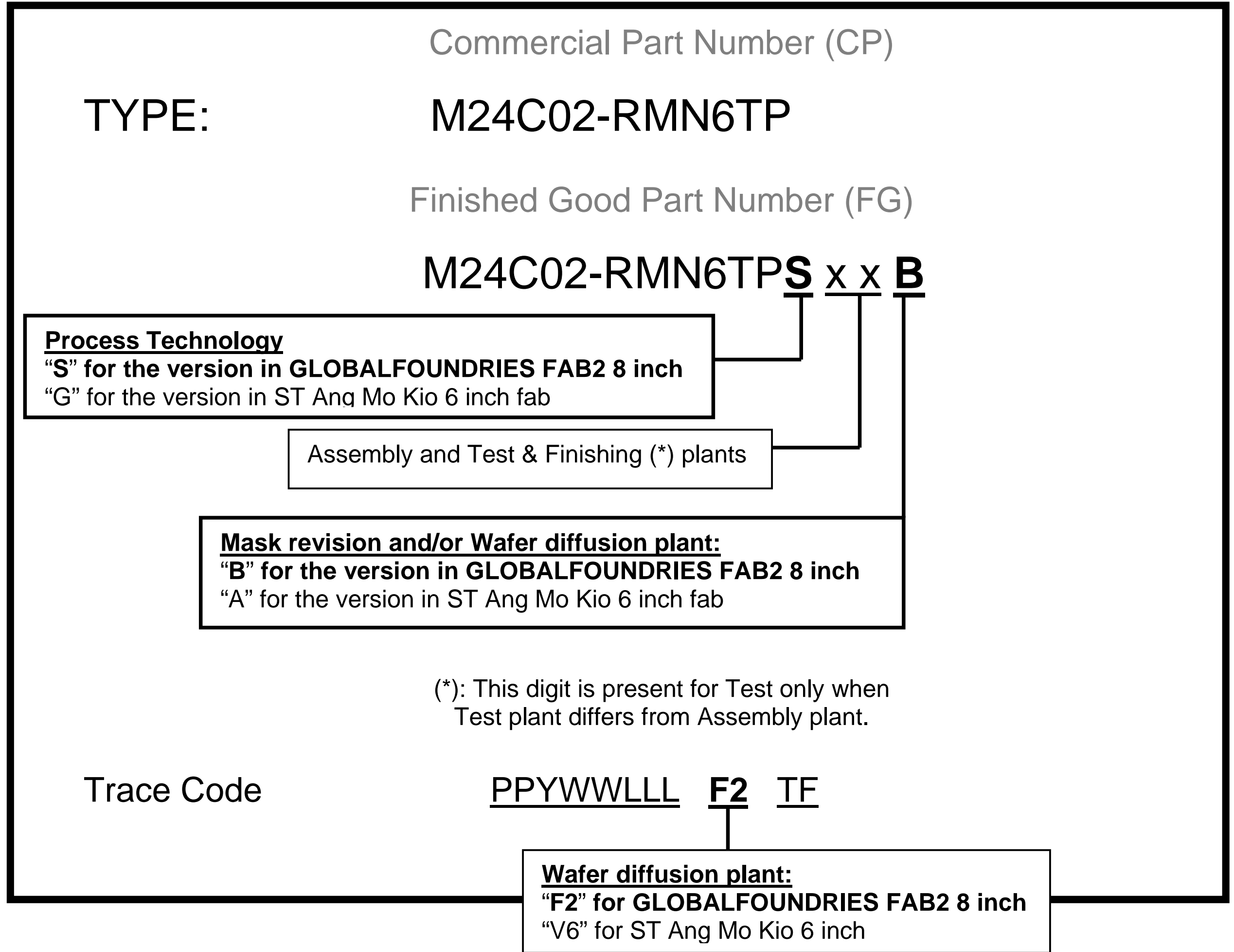
- BOX LABEL MARKING :

On the **BOX LABEL MARKING**, the change is visible inside the **Finished Good Part Number**:

- The **Process Technology** identifier is "**S**" for the **GLOBALFOUNDRIES** version, this identifier being "G" for the ST Ang Mo Kio version.
- The **Mask revision and/or Wafer diffusion plant** identifier is "**B**" for the **GLOBALFOUNDRIES** version, this identifier being "A" for the ST Ang Mo Kio version.

The change is also **visible** inside the **Trace Code**: the **Wafer diffusion plant** identifiers are "**F2**" for **GLOBALFOUNDRIES**, these identifiers being "V6" for the ST Ang Mo Kio.

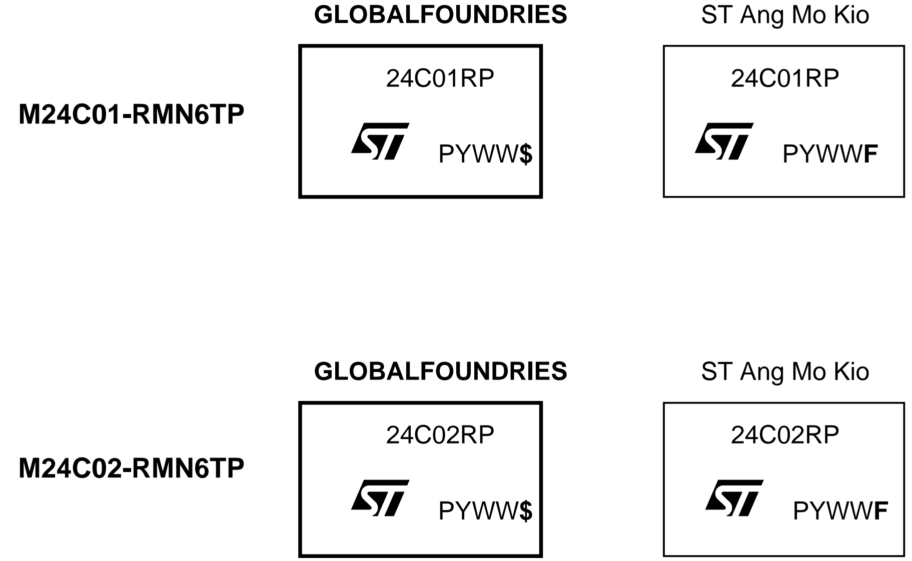
➔ *Example for M24C02-RMN6TP*



How can the change be seen?

- DEVICE MARKING :

On the **DEVICE MARKING** of the **SO8N**, the change is visible inside the Trace Code PYWWT where the **Process Technology identifier** “T” is “**$**” for Globalfoundries version, this identifier being “F” for ST Ang Mo Kio version.



Due to small sizes of **TSSOP8** and **MLP** packages, the change is not visible (see BOX LABEL MARKING in previous page).

Appendix A- Product Change Information

Product family / Commercial products:	M24C02-R & M24C01-R devices
Customer(s):	All
Type of change:	Wafer diffusion plant change
Reason for the change:	Wafer fab second source
Description of the change:	GLOBALFOUNDRIESFAB2, additional wafer fab for M24C02-R & M24C01-R devices
Forecast date of the change:	Week 33 / 2010
Forecast date of Qualification samples availability for customer(s):	Available
Forecast date for the internal STMicroelectronics change, Qualification Report availability:	QREE0825 is available and included inside this document (See APPENDIX C)
Marking to identify the changed product:	Process and fab ID see marking above
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See APPENDIX B
Manufacturing location:	GLOBALFOUNDRIES 8 inch wafer fab
Estimated date of first shipment:	Week 46 / 2010

Appendix B: List of affected products:

47-707129
M24C01-RDW6TP
M24C01-RMN6TP
M24C02-GRST01
M24C02-RDW6TP
M24C02-RMC6TG
M24C02-RMN6TP

Appendix C: Qualification Report:

QREE0825
Qualification report

New design / M24C01-R, M24C02-R, M34E02-F, M34C02-R using the CMOSF6SP36% DM technology at GlobalFoundries F2 8" Fab

Table 1. Product information

General information		
Commercial product	M24C01-RMN6TP M24C01-RDW6TP M24C02-RMN6TP M24C02-RDW6TP M24C02-RMC6TG	M34E02-FDW6TP M34E02-FMC6TG M34E02-FDW1TP M34C02-RDW6TP
Product description	– M24C01: 1 Kbit serial I²C bus EEPROM – M24C02: 2 Kbit serial I²C bus EEPROM – M34E02: 2 Kbit serial I²C bus EEPROM with permanent and reversible, software write protection – M34C02: 2 Kbit serial I²C bus EEPROM with permanent software write protection	
Product group	MMS	
Product division	MMY - Memory	
Silicon process technology	CMOSF6SP36% DM	
Wafer fabrication location	Subcon GlobalFoundries F2 8", Singapore	
Electrical Wafer Sort test plant location	ST Ang Mo Kio, Singapore	

Table 2. Package description

Package description	Qualified assembly plant location	Qualified final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	Subcon Amkor P1, Philippines	Subcon Amkor P3, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	Subcon Amkor P1, Philippines	Subcon Amkor P3, Philippines
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines
	Subcon Amkor P3, Philippines	Subcon Amkor P3, Philippines

Reliability / Qualification assessment: PASS

August 2010 Rev 1 1/13

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1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new design M24C01-R, M24C02-R, M34E02-F and M34C02-R using the CMOSF6SP36% DM Silicon process technology at subcontractor GlobalFoundries F2 8" diffusion fab.

The voltage and temperature ranges covered by this document are:

- 1.7 to 5.5 V at –40 to 85 °C for M34E02-F devices
- 1.8 to 5.5 V at –40 to 85 °C for M24C01-R, M24C02-R and M34C02-R devices

The CMOSF6SP36% DM Single Poly Double Metal Silicon process technology has already been qualified and is in production at subcontractor GlobalFoundries F2 8" diffusion fab for EEPROM products. This document serves principally for the qualification of the named products, using the named process in the named diffusion fab.

1.2 Conclusion

The new design M24C01-R, M24C02-R, M34E02-F and M34C02-R using the CMOSF6SP36% DM Silicon process technology at subcontractor GlobalFoundries F2 8" diffusion fab have passed the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details on the reliability test results.

2 Device characteristics

Device description

The M24C02-R is a 2 Kbit serial I²C bus EEPROM and the M24C01-R is a 1 Kbit serial I²C bus EEPROM.

The M34E02 and M34C02 are 2 Kbit serial I²C bus EEPROMs with the following features:

- The M34E02 devices have permanent and reversible, software write protection in their first half (from location 00h to 7Fh)
- The M34C02 devices have permanent software write protection in their first half (from location 00h to 7Fh)

These features have been specifically designed for use in DRAM DDR2 DIMMs (dual interline memory modules) with serial presence detect (SPD).

These I²C-compatible, electrically erasable programmable read-only memory (EEPROM) devices are organized as 256 × 8 bits (M24C02-R, M34E02-F, M34C02-R) or 128 × 8 bits (M24C01-R).

Refer to the product datasheets for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products have been qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicle used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M34E02 (1)	CMOSF6SP36% DM	subcon GlobalFoundries F2 8"	CDIP8	Engi assy (2)

1. The M24C01, M24C02 and M34C02 devices are derived from the M34E02 device during test flow. Consequently, M34E02 reliability results are used to qualify all named products.
2. CDIP8 is a ceramic package used only for die-oriented reliability trials.

Package qualifications are mainly obtained by similarity. The product vehicle and silicon process technologies used for package qualification are presented in *Table 4*.

Table 4. Product vehicle used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24C02	CMOSF6SP36% DM	subcon GlobalFoundries F2 8"	SO8N	ST Shenzhen
M24C16 (1)	CMOSF6SP36% DM	subcon GlobalFoundries F2 8"	SO8N	subcon Amkor P1
		ST Ang Mo Kio 6"	TSSOP8	ST Shenzhen
		ST Ang Mo Kio 6"	UFDFPN8 (MLP8) 2 × 3 mm	ST Calamba
		ST Ang Mo Kio 6"	UFDFPN8 (MLP8) 2 × 3 mm	subcon Amkor P3
		subcon GlobalFoundries F2 8"		
M95160 (1)	CMOSF6SP36% DM	subcon GlobalFoundries F2 8"	SO8N	ST Shenzhen
			TSSOP8	subcon Amkor P1

1. Package qualification results of M95160/M24C16 are applicable (same silicon process technology, larger memory array).

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen / subcon Amkor P1 package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen / subcon Amkor P1 package-oriented tests
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba & subcon Amkor P3 package-oriented tests
- Qualification report QREE0824 summarizes the results of the trials that were performed to qualify the SO8N Green package in ST Shenzhen assembly line for the EEPROM products.
- Qualification report QREE0424 summarizes the reliability trials performed to qualify the Pb-free Nickel Palladium Gold pre-plated frame on SO8 narrow package in the Amkor assembly line, and it shows the results obtained.
- Qualification report QREE0705 summarizes the reliability trials performed to qualify the TSSOP8 package using the strip test line in the Shenzhen assembly line, and it shows the results.
- Qualification report QREE0502 summarizes the reliability trials performed to qualify the Lead-free Nickel Palladium Gold pre-plated frame on TSSOP8 package in the Amkor P1 assembly line, and it gives the results of the trials.
- Qualification report QREE0917 summarizes the reliability trials and results performed to qualify the UFDFPN8 (MLP8) 2 x 3 mm in Calamba assembly line for EEPROM products.
- Qualification report QREE0926 summarizes the reliability trials and results performed to qualify the UFDFPN8 (MLP8) 2 x 3 mm in subcontractor Amkor P3 assembly line for EEPROM products.
- Qualification report QREE0311 summarizes the reliability trials that were performed to qualify the CMOSF6SP36% DM Silicon process technology at subcontractor GlobalFoundries F2 8" diffusion fab, and it shows the results.

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M34E02 (2) Lot 1
EDR	High temperature operating life after endurance					
	AEC-Q100-005	1 Million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	1	1008 hrs	0/80
	Data retention after endurance					
	AEC-Q100-005	1 Million E/W cycles at 25 °C then: HTSL at 150 °C	80	1	1008 hrs	0/80
LTOL	Low temperature operating life					
	JESD22-A108	–40 °C, 6 V	80	1	1008 hrs	0/80
HTSL	High temperature storage life					
	AEC-Q100-005 JESD22-A103	Retention bake at 200 °C	80	1	1008 hrs	0/80
WEB	Program/erase endurance cycling + bake					
	Internal spec.	1 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	1	1 Million cycles / 48 hrs	0/80 (3)
ESD HBM	Electrostatic discharge (human body model)					
	AEC-Q100-002 JESD22-A114	C = 100 pF, R = 1500 Ω	27	1	N/A	Pass > 4000 V
ESD MM	Electrostatic discharge (machine model)					
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	6	1	N/A	Pass > 400 V
LU	Latch-up (current injection and overvoltage stress)					
	AEC-Q100-004 JESD78A	At maximum operating temperature (85 °C)	6	1	N/A	Class II Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. The M24C01, M24C02 and M34C02 devices are derived from the M34E02 device during test flow. Consequently, M34E02 reliability results are used to qualify all named products.
3. First rejects after 10 million cycles + bake.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen & subcon Amkor P1) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95160 / M24C16 (2)			M34E02/ M34C02/ M24C01/ M24C02
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020C	MSL1, peak temperature at 260 °C, 3 IReflow	345	3	N/A	0/345	0/345	0/345	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	−65 °C / +150 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	−55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
COLD	Cold test								
	ADCS No. 8122199	Functional test at -40 °C	500	1	N/A	-	-	-	0/500
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Package qualification results of M95160/M24C16 are applicable (same Silicon process technology, larger memory array).
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen & subcon Amkor P1)[1]

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95160 / M24C16 [2]			M34E02/ M34C02/ M24C01/ M24C02
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020C	MSL1, peak temperature at 260 °C, 3 IReflow	345	3	N/A	0/345	0/345	0/345	-
THB [3]	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC [3]	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +150 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK [3]	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25	-
AC [3]	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL [3]	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
COLD	Cold test								
	ADCS No. 8122199	Functional test at -40 °C	500	1	N/A	-	-	-	0/500
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500V	-	-	Pass >1500V

1. See Table 9: List of terms for a definition of abbreviations.
2. Package qualification results of M95160/M24C16 are applicable (same Silicon process technology, larger memory array).
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2x3 mm / ST Calamba & subcon Amkor P3) (1)

Test	Short test description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24C16 (2)			M34E02/ M34C02/ M24C01/ M24C02
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020C	MSL1, peak temperature at 260 °C, 3 IReflow	345	3	N/A	0/345	0/345	0/345	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	−65 °C / +150 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	−55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Package qualification results of M24C16 are applicable (same silicon process technology, larger memory array).
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78A: IC Latch-up test
- J-STD-020C: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)
COLD	Cold test

Document Revision History		
Date	Rev.	Description of the Revision
Aug. 11, 2010	1.00	First draft creation

Source Documents & Reference Documents		
Source document Title	**Rev.:**	**Date:**

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