PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-IPC/10/5986
Notification Date 10/25/2010

Additional BCD5 Technology Ang Mo Kio 6" wafers fab (AMK6) for Linear Voltage Regulator product

Table 1. Change Implementation Schedule

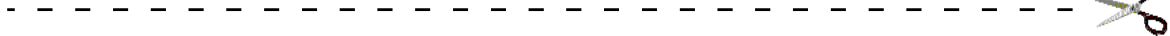
Forecasted implementation date for change	15-Jan-2011
Forecasted availabillity date of samples for customer	05-Nov-2010
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	18-Oct-2010
Estimated date of changed product first shipment	24-Jan-2011

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Waferfab additional location
Reason for change	Capacity rationalization and increase
Description of the change	At the aim to continuously improve our service and rationalize ST assets, we are expanding the production of BCD5 technology in Ang Mo Kio 6" facility, already qualified since 2008, and running in volumes for the last 2 years (see PCN APM-IPC/08/4269, dated December 29th 2008). So,the Linear Voltage Regulator products using the above technology, today diffused in AGRATE 8" fab (AG8), will be diffused also in Ang Mo Kio 6" (AMK6).
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	V6 are the digits used to identify AMK6 FAB in trace code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN APM-IPC/10/5986**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 10/25/2010**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Riviera, Antonio	Division Marketing Manager
Naso, Lorenzo	Division Product Manager
Motta, Antonino	Division Q.A. Manager

BCD5 PROCESS DIFFUSED IN AMK6 (6")

WHAT:
Following the BCD5 process qualification in AMK6 notified thru PCN APM-IPC/08/4269, dated December 29th 2008, please be informed that the Linear Voltage Regulator products using BCD5 Technology, currently manufactured in AGRATE 8" plant, will be also produced in our facilities located in Singapore Ang Mo Kio 6" plant. The affected products are listed in the attached table.

WHY:
To optimize ST asset utilization and enhance performance for Shareholders and Customers.

HOW:
Qualification will be run by extension of 2008 qualification results (see PCN APM-IPC/08/4269, dated December 29th 2008) and qualification data of product belonging to the same Division (L5973D, DC-DC Converter), run of pilot lots for the highest runner Voltage Regulator device (LD39150PTR) and comparison of electrical performance between the original and the new source (by T84, EWS data, electrical characterization data).
New source material will keep the original electrical, dimensional and thermal parameters for the affected product, maintaining unchanged the current information published on the relevant datasheets. There are no changes in the packing modes or in the standard delivery quantities either.

WHEN:
The availability of all product lines and the ramp up in the new location will be finalized within Q4 2010.

Samples availability:
Samples of P/N LD39150PTR, will be available by wk46 2010. For other P/Ns, samples will be made available upon request.

Change implementation schedule:
The production start and first shipments will be implemented according to our work in progress and materials availability as indicated in the schedule below:

Product Family Code	Product Family Description	1st Shipments
32	Linear Voltage Regulator	From Week 4 2011

Product's traceability:
Unless otherwise stated by customer specific requirement, new parts produced in AMK 6" Singapore will be differentiated as indicated below:

Diffusion plant	ID	Country of origin
AGRATE AG8 (current)	V1	Italy
ANG MO KIO AMK6 (new)	V6	Singapore

Shipments from new Wafer FAB location will be tracked on the ST Standard Label as showed below:

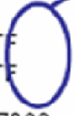
Manufactured under patents or patents pending

STMicroelectronics

Assembled in: 1234567890123456
Pb-free 2nd Level Interconnect
MSL: 12 Bag seal date: dd mm yyyy
PBT: 260 C Category: xx ECOPACK/RoHS

TYPE: 1234567890123456
1234567890123456

Total Qty: 12345

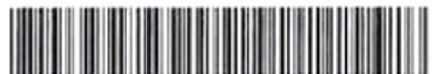


Trace codes PPYWWLL1 WX TF
PPYWWLL2 WX TF

Wafer FAB area code will change
from: V1
to: V6

Marking 12345678901234567890

Bulk ID 1234567890123



Please provide the bulk ID for any inquiry

Generic ST Standard label

Reliability Report

General Information	
Product Line	*UD73 EC6*
Product Description	*2.5A SWITCH STEP DOWN SWITCHING REGULATOR*
Product division	*I&PC*
Package	*HSOP 8L*
Silicon process technology	*BCD5-44NP*

Locations	
Wafer fab location	*ANG MO KIO*
Assembly plant location	*AMKOR ATP1 PHILIPPINES*
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	19-Feb-09	10	M. Benzoni	Original document

Issued by

Massimo Benzoni

Reviewed by

Alceo Paratore

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
SOP 2.6.10	: General product qualification procedure
SOP 2.6.11	: Program management fro product qualification
SOP 2.6.12	: Design criteria for product qualification
SOP 2.6.14	: Reliability requirements for product qualification
SOP 2.6.19	: Process maturity level
SOP 2.6.2	: Process qualification and transfer management
SOP 2.6.20	: New process / New product qualification
SOP 2.6.7	: Product maturity level
SOP 2.6.9	: Package and process maturity management in Back End
SOP 2.7.5	: Automotive products definition and status

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of UD73 EC6 device diffused in ANG MO KIO and assembled in HSOP 8L in AMKOR ATP1 PHILIPPINES.
According to Reliability Qualification Plan, below is the list of the trials performed:

Die Oriented Tests

- High temperature Operating Life
- High Temperature Reverse Bias
- Temperature Humidity Bias

Package Oriented Tests

- Preconditioning
- Temperature Cycling
- Autoclave
- High Temperature Storage Life
- Temperature Humidity Storage

Electrical Characterization

- ESD resistance test
- LATCH-UP resistance test

2.2 Conclusion

Taking in account the results of the trials performed **the UD73 EC6 diffused in ANG MO KIO and assembled in HSOP 8L in AMKOR ATP1 PHILIPPINES can be qualified from reliability viewpoint.**

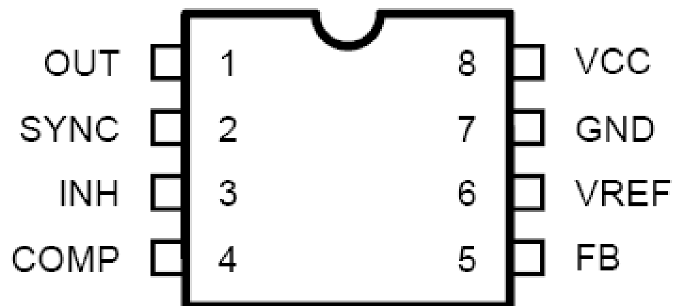
3 DEVICE CHARACTERISTICS

3.1 Device description

3.1.1 Generalities

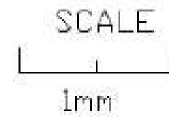
The L5973D is a step down monolithic power switching regulator with a minimum switch current limit of 2.5A so it is able to deliver more than 2A DC current to the load depending on the application conditions. The output voltage can be set from 1.235V to 35V.

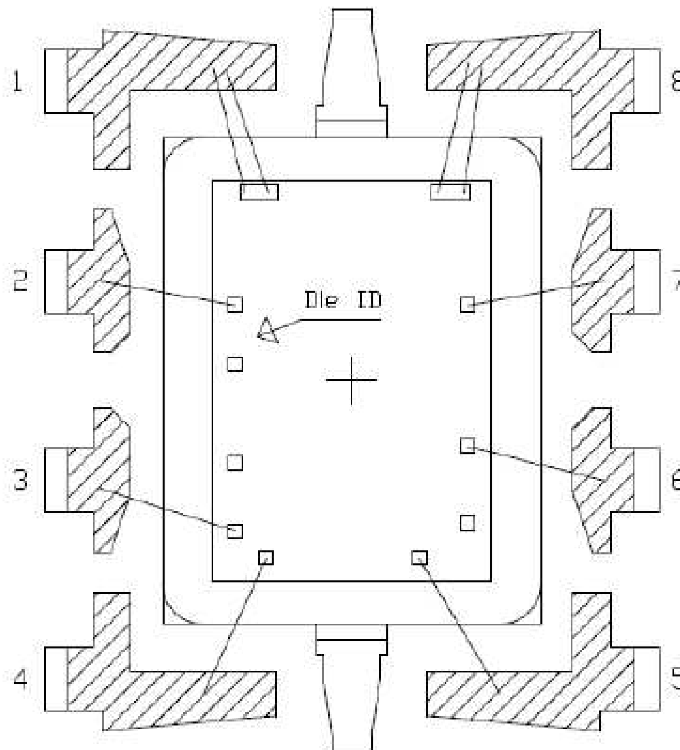
3.1.2 Pin connection



3.1.3 Bonding diagram

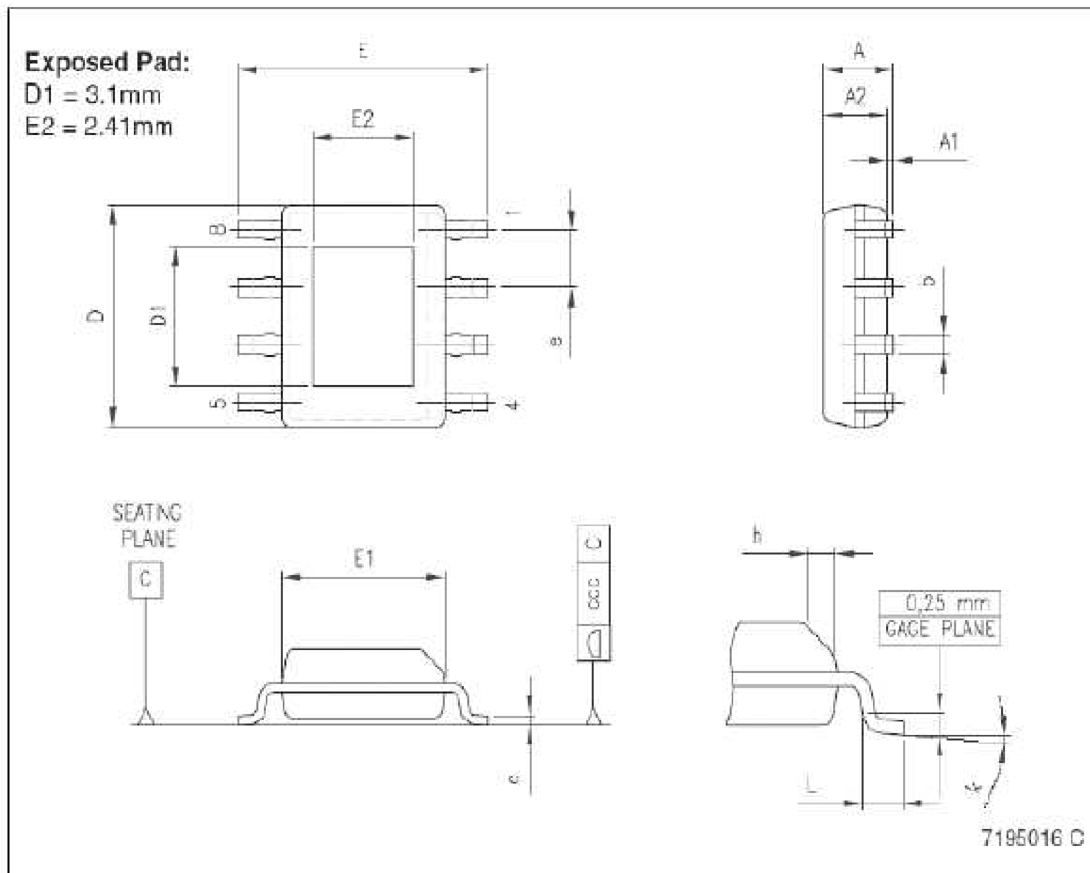
FRAME PAD : .095 x .122 inch
2,413 x 3,099 mm





3.1.4 Package outline/Mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.70			0.0669
A1	0.00		0.15		0.00	0.0059
A2	1.25			0.0492		
b	0.31		0.51	0.0122		0.0201
c	0.17		0.25	0.0067		0.0098
D	4.80	4.90	5.00	0.1890	0.1929	0.1969
E	5.80	6.00	6.20	0.2283		0.2441
E1	3.80	3.90	4.00	0.1496		0.1575
e		1.27				
h	0.25		0.50	0.0098		0.0197
L	0.40		1.27	0.0157		0.0500
k	0		8			0.3150
ccc			0.10			0.0039



3.2 Traceability

Wafer fab information	
Wafer fab manufacturing location	*ANG MO KIO*
Wafer diameter	*6 inches*
Wafer thickness	*375 µm*
Silicon process technology	*BCD5-44NP*
Die finishing back side	*Cr/Ni*
Die size	*2770x1980 µm*
Bond pad metallization layers	*AlSiCu*
Passivation	*SiON + PIX*
Metal levels	*3*

Assembly Information	
Assembly plant location	*AMKOR ATP1 PHILIPPINES*
Package description	*HSOP8*
Die pad size	*2.413x3.099 mm*
Molding compound	*Ablebond 8290*
Wires bonding materials/diameters	*Au/1.3 mils*
Die attach material	*Sumitomo G600*
Lead solder material	*Sn*

4 TESTS RESULTS SUMMARY

4.1 Test plan and results summary

Die Oriented Tests						
Test	**Method**	**Conditions**	**Sample/ Lots**	**Number of lots**	**Duration**	**Results Fail/SS**
HTRB	High Temperature Reverse Bias	**Tj=150°C, Vcc=40V**	**77**	3	**1000h**	**0/231**
HTOL	High Temperature Operating Life On chip board	**Tj=150°C** **Vcc=36V, Iout=2A**	**77**	3	**1000h**	**0/231**
THB	Temperature Humidity Bias					
	PC Before	**Ta=85°C, HR=85%** **Pdut~0W, Vcc=20V**	**40**	1	**1000h**	**0/40**

Package Oriented Tests						
Test	**Method**	**Conditions**	**Sample/ Lots**	**Number of lots**	**Duration**	**Results Fail/SS**
PC	Pre-Conditioning: Moisture sensitivity level 3					
		192h 30°C/60% - Jedec 020C	**200**	1		**0/200**
AC	Autoclave					
	PC before	**121°C 2atm**	**77**	1	**168h**	**0/77**
TC	Temperature Cycling					
	PC before	**Temp. range: -50/+150°C**	**77**	1	**1000cy**	**0/77**
HTSL	High Temperature Storage					
	No bias	**Tamb=150°C**	**77**	1	**1000h**	**0/77**
THS	Temperature Humidity Storage					
	No Bias	**Tamb=85°C, RH=85%**	**77**	1	**1000h**	**0/77**

Electrical Characterization Tests						
Test	**Method**	**Conditions**	**Sample/ Lots**	**Number of lots**	**Duration**	**Results Fail/SS**
ESD	Electro Static Discharge					
	Human Body Model	**+/- 2500V**	**3**	1		**0/3**
	Charge Device Model	**+/- 1500V**	**3**	1		**0/3**
LU	Latch-Up					
	Over-voltage and Current Injection	**Tamb=125°C** **Jedec78 – Level B**	**3**	1		**0/3**

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing @ 1000 hrs @ Ta=25°C

5.1.2 High Temperature Reverse Bias

This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs @ Ta=25°C
- Final Testing @ 1000hrs @ Ta=25°C

5.1.3 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed is static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions Ta=85°C / RH=85% .
Inputs pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 1000h

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs @ Ta=25°C
- Final Testing @ 1000hrs @ Ta=25°C

5.2 Package oriented tests

5.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance.
The typical failure modes are "pop corn" effect and delamination.

5.2.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.2.3 Temperature Humidity Storage

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chard is the following:

- Initial testing @ Ta=25°C.
- Readout @ 500hrs
- Final Testing @ 1000hrs @ Ta=25°C.

TEST CONDITIONS:

- Ta= 85°C
- RH= 85%
- test time= 1000 hrs

5.2.4 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 500 cycles.
- Final Testing @ 1000 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -50°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.2.5 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing @ 168hrs @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168hrs

5.3 Electrical Characterization Tests

5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low: 0V	-80mA	Inom+200mA	Vcc=46V
IN high: 4.0V	-50mA	Inom+200mA	Vcc=46V

5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** JEDEC STANDARD JESD22-A114
  CDF-AEC-Q100-002
- **Charge Device Model** JEDEC STANDARD JESD22-C101
  CDF-AEC-Q100-011

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