PRODUCT/PROCESS CHANGE NOTIFICATION

TITLE	**L9616-TR, L9616 (UB62): Assembly Transfer to Bouskoura**
IMPACTED PRODUCTS	- L9616-TR - L9616
MANUFACT. STEP	Assembly
INVOLVED PLANT	Recipient: ST Shenzhen Plant (China) Destination: ST Bouskoura Plant (Morocco)
CHANGE REASON	Service and Capacity improvement. Manufacturing process optimization.
CHANGE DESCRIPTION	Transfer of package assembly from current Shenzhen (China) to Bouskoura (Morocco) Plant. Package Bill of Material is subject to upgrade as per following table:
TRACEABILITY	Dedicated Finished Good Codes (internal part number)
VALIDATION	According to ZVEI Delta Qualification Matrix corresponding to following selected items: - SEM-PA-04 Change of lead frame finishing material / area (internal) - SEM-PA-08 Change of wire bonding - SEM-PA-18 Move all or parts of production to a different assembly site leading to the reliability qualification plan and report enclosed.
CURRENT PRODUCTS	Replaced by new version featuring new Plant and upgraded package
REPORTS	14096 Validation.pdf (Report RR007622CS2039_01)

	SHENZHEN	BOUSKOURA	Notes
GLUE	ABLESTIK 8601S-25	ABLESTIK 8601S-25	same
FRAME	94x125 Mt HD NiThPdAgAu	94x125 SSHD IDF SpAg	different
LEAD FINISHING	e4	e3	different
RESIN	SUMITOMO EME-G700KC	SUMITOMO EME-G700KC	same
WIRE	Au D1.0	Cu D1.0	different

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : L9616-TR, L9616 (UB62): Assembly Transfer to Bouskoura

PCN Reference : ADG/23/14096

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

L9616-TR	L9616	

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Choose an item.

RELIABILITY EVALUATION REPORT

SO8 package

Assy plant transfer from Shenzhen to Bouskoura and new BOM introduction

General Information	
Commercial Product	*L9856* *L9637* *L4979D*
Product Line	*U356-BA6* *U537-BD6* *UH01-BB6*
Product Description	*High voltage high-side driver* *Monolithic bus driver* *Low dropout linear regulator*
Package	*SO8*
Silicon Technology	*BCD*
Division	*SPS*

Traceability	
Diffusion Plant	*AMK - Singapore*
Assembly Plant	*Bouskoura - Morocco*
Passed	*X*

Disclaimer: *this report is a summary of the qualification plan results performed in good faith by STMicroelectronics to evaluate the electronic devices conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party, except in full, without previous written agreement by STMicroelectronics or under the approval of the author (see below)*

REVISION HISTORY

Version	Date	Author	Changes description
1.0	29th August 2022	G. Germani	First release

APPROVED BY: D. BINI

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

Aim of this report is to describe the results of the reliability activity performed to evaluate the assy plant transfer from Shenzhen to Bouskoura with the new BOM introduction (SSHD SpAg frame + Copper wires) for BCD products:

- U356-BA6 (L9856) a high voltage high-side driver, assembled in SO-8 package and diffused in BCD Offline
- U537-BD6 (L9637), a monolithic bus driver, assembled in SO-8 package and diffused in BCD2
- UH01-BB6 (L4979D), a low dropout linear regulator, assembled in SO-8 package and diffused in BCD4

The evaluation has been carried out on three independent wafer lots assembled, for each product, in three independent (non-consecutive) assy lots.

Details are reported in the next pages.

1.2 Reliability Test Plan

Reliability tests performed on this device are in agreement with **ST 0061692** and **AEC Q100 rev H** specification and are listed in the Test Plan (see below Table 1).
For details on test conditions, generic data used and spec reference see test results summary at Par.3 and 4.

1.2.1 Test Plan

TABLE 1

TEST GROUP	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
A Accelerated Environment Stress	**PC (JL3)**	Preconditioning (MSL3+3 reflow simulation+100 TC)	Y
	THB (or HAST)	Temperature Humidity Bias	Y
	AC (or UHAST or THS)	Autoclave at 2atm	Y
	TC	Temperature Cycling	Y
	PTC	Power Temperature Cycling	Y
	HTSL	High Temperature Storage Life	Y
B Accelerated Environment Stress	**HTOL**	High Temperature Operating Life	Y
	ELFR	Early Life Failure Rate	Y
	EDR	Electrical Data Retention for NVM	NA
C Package Assembly Integrity	**WBS**	Wire Bond Shear	Y
	WBP	Wire Bond Pull	Y
	SD	Solderability	Y
	PD	Physical Dimension	Y
	SBS	Solder Ball Shear	NA
	LI	Lead Integrity	NA
E Electrical Verification	**ESD (HBM)**	Electrostatic Discharge (Human Body Model)	NA
	ESD (CDM)	Electrostatic Discharge (Charged Device Model)	NA
	LU	Latch Up	NA
	ED	Electrical distribution	Y
	FG	Fault grade	NA
	CHAR	Characterization	NA
	EMC	Electromagnetic Compatibility	NA
	SC	Short Circuit Characterization	NA
	SER	Soft Error Rate	NA
	LF	Lead (Pb) Free: (see AEC-Q005)	Y
D Die Fabrication Reliability	Test list is reported in AEC-Q100 table at Par.4	Performed during process qualification	N
F Defect Screening	Test list is reported in AEC-Q100 table at Par.4	To be implemented starting from first production lot	Y
G Cavity Package Integrity	Test list is reported in AEC-Q100 table at Par.4	Not for plastic packaged devices	NA

1.2.1 Additional Test Plan

TABLE 2

TEST GROUP	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
H Tests no Q100	**HTRB**	High Temperature Reverse Bias	Y

Flag Legenda: Y = Done
N = Not done
S = Similarity (Generic Data)
NA = Not Applicable

1.3 Conclusion

All reliability tests have been completed with positive results.
Neither functional nor parametric rejects were detected at final electrical testing.
Parameter drift analysis performed on samples submitted to die oriented tests (HTOL, PTC and HTRB) showed a good stability of the main electrical monitored parameters.
Package oriented tests have not put in evidence any criticality.
Physical analyses have not put in evidence any issue.

On the basis of the overall results obtained, we can give a positive judgment on the reliability evaluation of U356-BA6, U537-BD6 and UH01-BB6, diffused in BCD Offline, BCD2 and BCD4 (AMK Singapore) and assembled in SO8 package (ST Bouskoura - Morocco), performed in agreement with AEC_Q100 Rev. H specification Grade 1 and Q006.

2 DEVICE CHARACTERISTICS

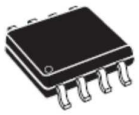
2.1 U356 Generalities

The L9856 is an high voltage device, manufactured with the BCD "OFF-LINE" technology.

It has the capability of driving N-Channel Power MOS transistors. The upper (floating) section is enabled to work with voltage rail up to 160 V. The logic Inputs are CMOS/TTL compatible for ease of interfacing with controlling devices.

Features

- High voltage rail up to 160 V
- dV/dt immunity ±50 V/nsec in full temperature range
- Driver current capability:
  500 mA source,
  500 mA sink
- Switching times 100 ns rise/fall with 2.5 nF load
- CMOS/TTL Schmitt trigger inputs with hysteresis
- Under voltage lock out
- Clamping on V_{CC}
- Loading circuit for external Bootstrap capacitor
- Inverting input
- Reset circuitry
- SO-8 package

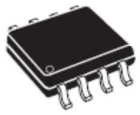


2.2 U537 Generalities

The L9637 is a monolithic integrated circuit containing standard ISO 9141 compatible interface functions.

Features

- Operating power supply voltage range $4.5\ V \le V_S \le 36\ V$ (40 V for transients)
- Reverse supply (battery) protected down to $V_S \ge -24\ V$
- Standby mode with very low current consumption $IS_{SB} \le 1\ mA$ @ $V_{CC} \le 0.5\ V$
- Low quiescent current in off condition $IS_{OFF} = 120\ \mu A$
- TTL compatible TX input
- Bidirectional K-I/O pin with supply voltage dependent input threshold
- Overtemperature shut down function Selective to K-I/O pin
- Wide input and output voltage range $-24\ V \le V_K \le V_S$
- K output current limitation, typ. $I_K = 60\ mA$
- Defined OFF output status in undervoltage condition and V_S or GND interruption
- Controlled output slope for low EMI
- High input impedance for open V_S or GND connection
- Defined output ON status of LO or RX for open LI or K inputs
- Defined K output OFF for TX input open
- Integrated pull up resistors for TX, RX and LO
- EMI robustness optimized

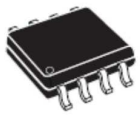


2.3 UH01 Generalities

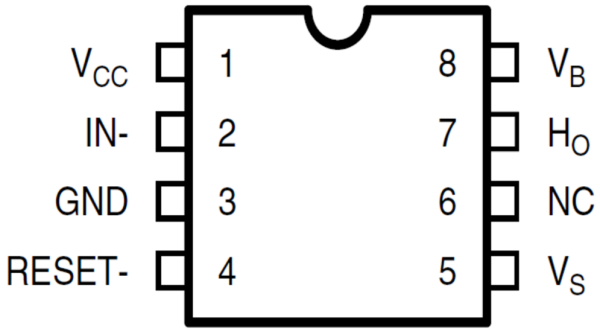
L4979D is a low dropout linear regulator with microprocessor control functions such as low voltage reset, watchdog, on/off control. Typical quiescent current is 100 microA in very low output current mode and enabled regulator. The device drop to 6 microA with not enabled regulators.
On chip trimmimg results in high output voltage accuracy (+/-2%). Accuracy is kept over wide temperature range, line and load variation.
The maximum input voltage is 40V. The max output current is internally limited. Internal temperature protection disables the voltage regulator output.

Features

- AEC-Q100 qualified
- Operating DC supply voltage range 5.6 V to 31 V
- Low quiescent current (6 µA typ. @ 25 °C with enable low)
- High precision output voltage (+/-2%)
- Low dropout voltage less than 0.5 V
- Reset circuit sensing the output voltage down to 1 V
- Programmable reset pulse delay with external capacitor
- Watchdog
- Programmable watchdog timer with external capacitor
- Thermal shutdown and short circuit protection
- Automotive temperature range (T_j = -40 °C to 150 °C)
- Enable input for enabling/disabling the voltage regulator output

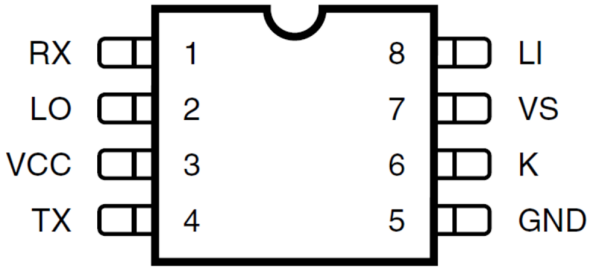


2.4 U356 Pin connections



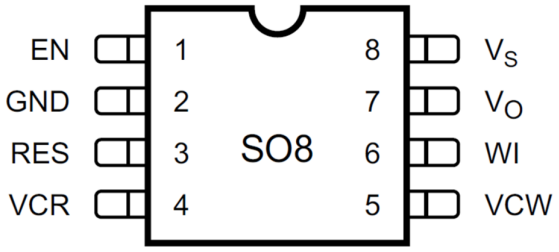
Pin #	Pin name	Description
1	V_{CC}	Driver supply, typical 5V
2	IN-	Driver control signal input (negative logic)
3	GND	Ground
4	RESET-	Driver enable signal input (negative logic)
5	V_S	MOSFET source connection
6	NC	No connection (no bondwire)
7	H_O	MOSFET gate connection
8	V_B	Driver output stage supply

2.5 U537 Pin connections



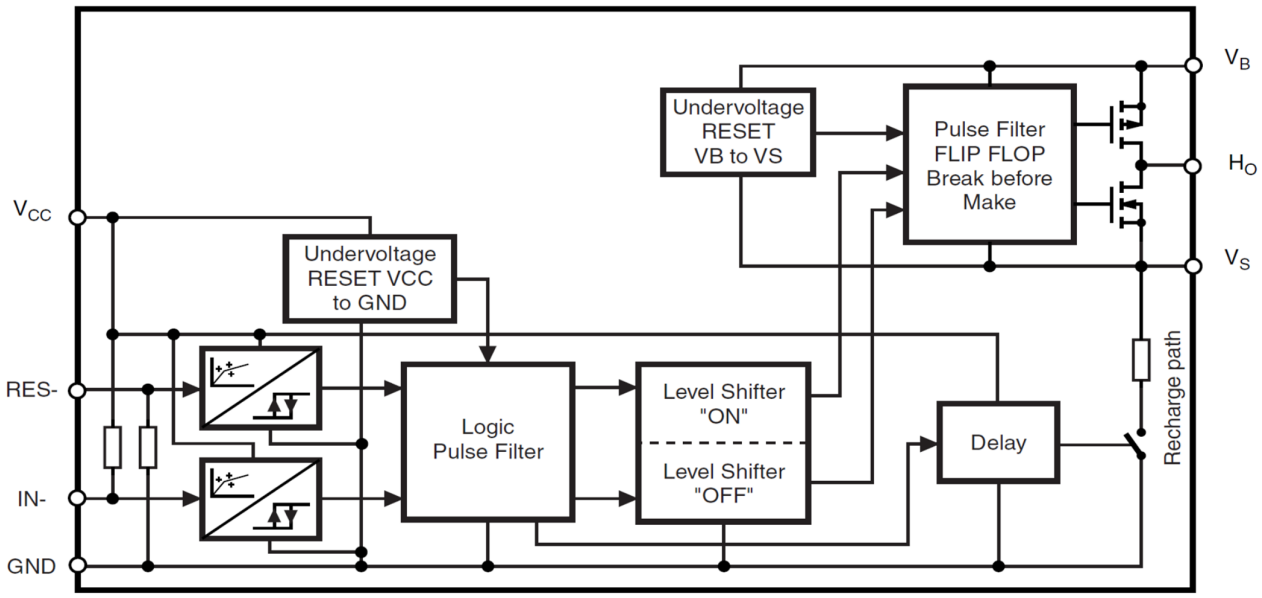
N.	Name	Function
1	RX	Output for K as input
2	LO	Output L comparator
3	VCC	Stabilized voltage supply
4	TX	Input for K as output
5	GND	Common GND
6	K	Bidirectional I/O
7	VS	Supply voltage
8	LI	Input L comparator

2.6 UH01 Pin connections

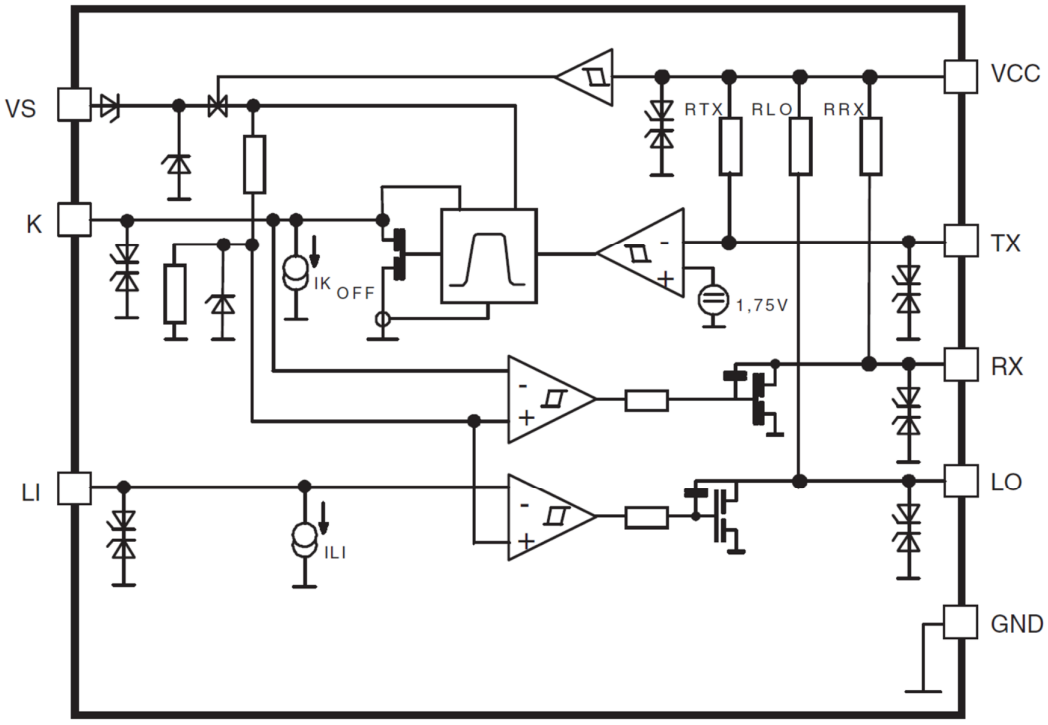


SO8 pin number	Pin name	Function
1	En	Enable input If high, regulator, watchdog and reset are operating. If low, regulator, watchdog and reset are shut down.
2	gnd	Ground reference
	gnd	Ground. These pins are to be connected to a heat spreader electrically grounded
3	Res	Reset output. It is pulled down when output voltage drops below V_{o_th} or frequency at W_i is too low.
4	Vcr	Reset timing adjust a capacitor between Vcr pin and gnd sets the reset delay time (t_{rd})
5	Vcw	Watchdog timer adjust a capacitor between V_{cw} pin and gnd sets the time response of the watchdog monitor.
6	Wi	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.
7	Vo	Voltage regulator output Output capacitor >100 nF is needed for regulator stability
8	Vs	Supply voltage Supply capacitor (e.g. 200 nF) is needed for regulator stability.

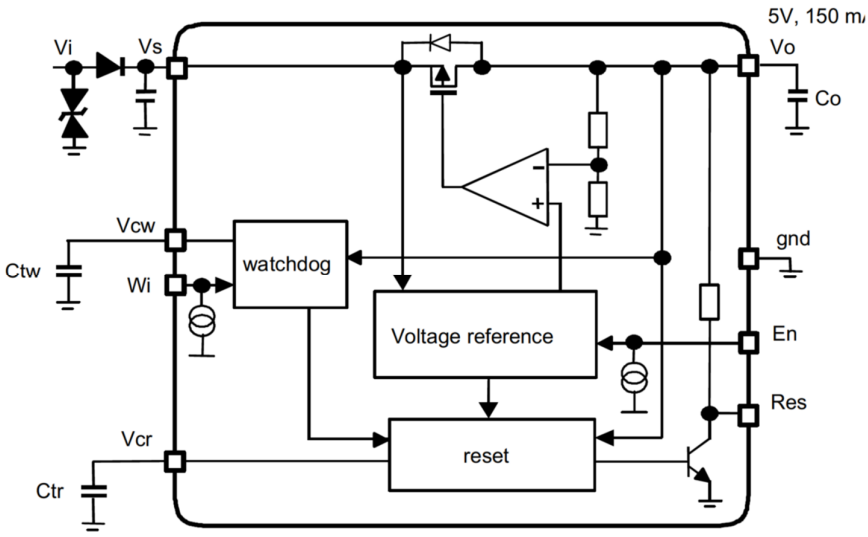
2.7 U356 Block diagram



2.8 U537 Block diagram



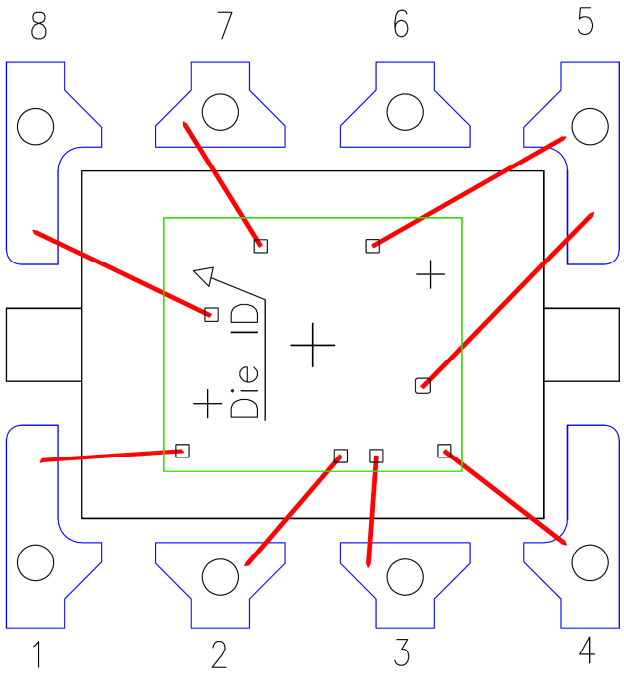
2.9 UH01 Block diagram



2.10 U356 Bonding diagram

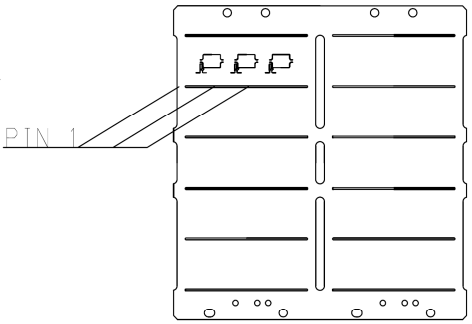
BONDING DIAGRAM FOR LINE : U356 IN SO8 OPT B SSHD Bouskoura

FRAME PAD : 94 x 125 mils / 2,388 x 3,175 mm



BONDING LEAD'S AREA

SO 8L 94x125 SSHD IDF 600u OpB SpAg , Ref DM00366324
FRAME CODE: 5FT70577
REMARK: E.S.D. PROGRAM IS MANDATORY
100% BALL CENTERING IS MANDATORY.

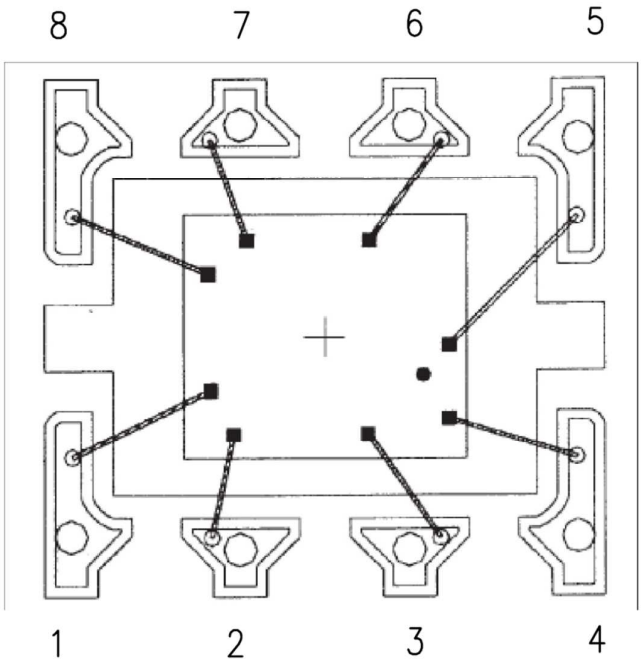


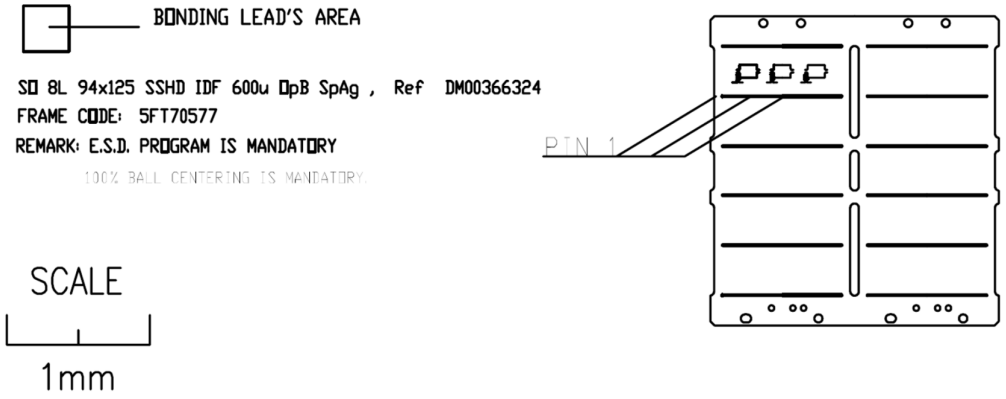
SCALE
1mm

2.11 U537 Bonding diagram

BONDING DIAGRAM FOR LINE : U537 IN SO8 OPT B SSHD BOUSKOURA

FRAME PAD : 94 x 125 mils / 2,388 x 3,175 mm

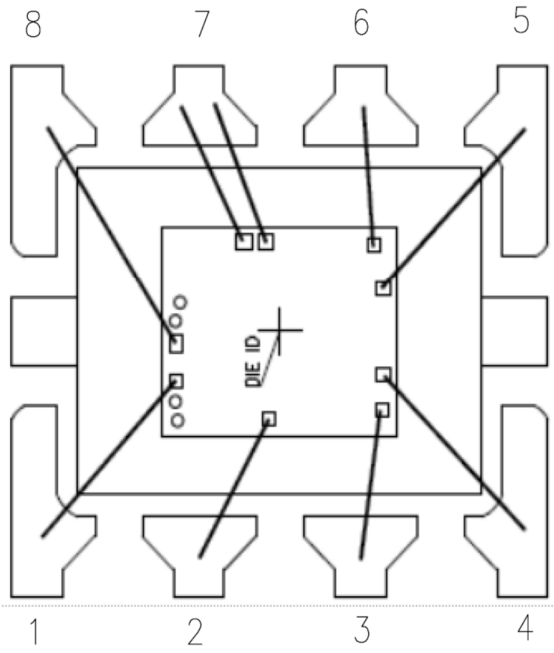


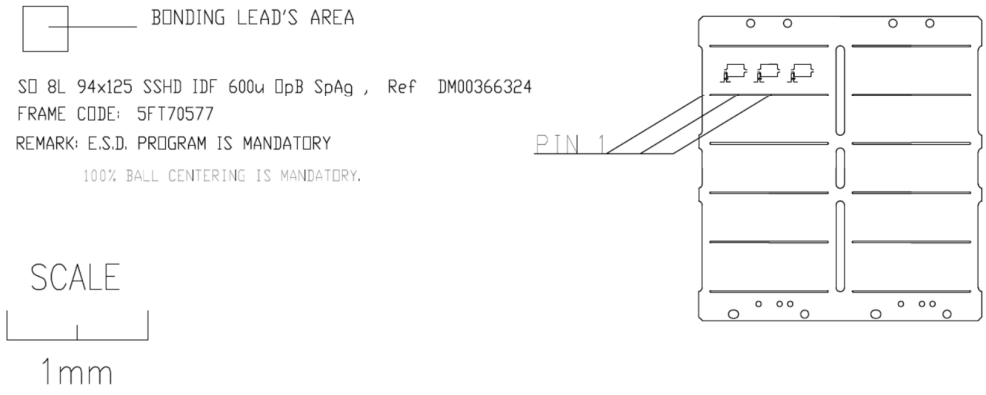


2.12 UH01 Bonding diagram

BONDING DIAGRAM FOR LINE : UH01 IN SO8 OPT B SSHD Bouskoura

FRAME PAD : 94 x 125 mils / 2,388 x 3,175 mm





2.13 Traceability

2.13.1 Wafer fab information

Wafer fab information			
	U356	**U537**	**UH01**
Wafer fab manufacturing location	AMK Singapore	AMK Singapore	AMK Singapore
Wafer diameter (inches)	6”	6”	6”
Silicon process technology	BCD Offline	BCD2	BCD4
Die finishing front side (passivation)	SiN	SiN	USG / PSG / SiON / PIX
Die finishing back side	Lapped silicon	Cr / Ni / Au	Raw silicon
Die area (Stepping die size)	2200 µm, 1900 µm	1860 µm, 2150 µm	1700 µm, 2010 µm
Metal levels / Materials	Metal 1: AlSiCu	Metal 1: AlSiCu Metal 2: AlSiCu	Metal 1: AlSiCu Metal 2: AlSiCu

2.13.2 Assembly information

Assembly Information	
	U356 / U537 / UH01
Assembly plant location	ST Bouskoura 2– Morocco
Package code description	SO8
Leadframe / Substrate	SO 8L 94x125 SSHD IDF 600uOpB SpAg
Die attach material	LOCTITE ABLESTIK 8601S-25 10cc/32g
Wires bonding materials/diameters	Cu 1.0 mil
Molding compound	SUMITOMO EME-G700KC D16mm W8.8g

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Product	Lot	Corner	Diffusion Lot	Trace Code	Raw Line
U356	1	NN	V60473Y8	CZ11703S	SSO7*U356BA6
	2	HH	V60473Y8	CZ1180AB	
	3	LL	V60473Y8	CZ1190AV	
U537	4	NN	V6109NFH	CZ1210J5	SSO7*U537BD6
	5	HH	V6109NFH	CZ12207K	
	6	LL	V60063NX	CZ1250J5	
UH01	7	NN	V60035VY	CZ10206L	SSO7*UH01BB6
	8	HH	V60046V3	CZ10303Y	
	9	LL	V60046V7	CZ10406P	

3.2 Test results summary

Test plan results are summarized in the Q100 Rev.H Template.
In Test Conditions column are also reported Electrical Temp and Physical Analysis required by AEC spec (**in bold**) and any additional STM requirements.
Test method revision reference is the one active at the date of reliability test trial.

3.2.1 Test results summary (Q100 Rev.H)

Test	#	Reference	Q100/STM Test Conditions	Lots	S.S.	Total	Results Lot/Fail/S.S.	Comments: (N/A =Not Applicable)
TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS								
PC	A1	JESD22 A113 J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C ☒ Testing at Room (pre) * ☒ Testing at Cold (pre)* ☒ Testing at Hot (pre)* ☒ 100 TC after reflow * Post test temp according to subsequent test requirement	APPLIED MSL = JL3			PASS	Before HTOL, PTC, THB, AC, TC, HTRB
THB	A2	JESD22 A101	Ta=85°C, 85%RH, Duration = 1000 h Robustness = 2000 h ☒ After PC ☒ Testing at Room ☒ Testing at Hot ☒ C-SAM post ☒ WBP (first / second bond) ☒ WBS ☒ Internal Inspection ☒ Cross section	6	77	462	Lot 1:0/77 Lot 2:0/77 Lot 4:0/77 Lot 7: 0/77 Lot 8: 0/77 Lot 9: 0/77	Physical analysis as per Q006 positively completed

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
AC	A3	JESD22 A102	P=2.08atm Ta=121°C, Duration = 96 h ☒ After PC ☒ Testing at Room ☒ Internal Inspection	9	77	693	Lot 1: 0/77 Lot 2:0/77 Lot 3:0/77 Lot 4: 0/77 Lot 5:0/77 Lot 6:0/77 Lot 7: 0/77 Lot 8: 0/77 Lot 9: 0/77	Physical analysis positively completed
TC	A4	JESD22 A104	Ta=-55°C /+150 °C Duration= 1000 cy Robustness = 2000 cy ☒ After PC ☒ Testing at Room ☒ Testing at Hot ☒ C/T-SAM post ☒ WBP ☒ WBS ☒ Internal Inspection ☒ cross section	9	77	693	Lot 1: 0/77 Lot 2:0/77 Lot 3:0/77 Lot 4: 0/77 Lot 5:0/77 Lot 6:0/77 Lot 7: 0/77 Lot 8: 0/77 Lot 9: 0/77	Physical analysis as per Q006 positively completed
PTC	A5	JESD22 A105	Ta=-40°C / Tj=+150 °C Duration= 1000 cy Robustness = 2000 cy ☒ After PC ☒ Testing at Room ☒ Testing at Hot ☒ Drift Analysis	1	45	45	Lot 8. 0/45	No significant drift observed in drift analysis
HTSL	A6	JESD22 A103	Ta= 150ºC Duration = 1000 h Robustness = 2000 h ☒ Testing at Room ☒ Testing at Hot ☒ WBP ☒ cross section	9	45	405	Lot 1: 0/45 Lot 2:0/45 Lot 3:0/45 Lot 4: 0/45 Lot 5:0/45 Lot 6:0/45 Lot 7: 0/45 Lot 8:0/45 Lot 9:0/45	Physical analysis as per Q006 positively completed

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

HTOL	B1	JESD22 A108	Tj=150°C Duration= 1000 hrs ☒ Testing at Room ☒ Testing at Cold ☒ Testing at Hot ☒ Drift Analysis	3	77	231	Lot 1: 0/77 Lot 7: 0/77 Lot 9: 0/77	No significant drift observed in drift analysis
ELFR	B2	AEC-Q100-008	Burn-in conditions with Tj=150°C (Ta max=125C) Duration=48 hrs ☒ Testing at Room ☒ Testing at Hot	3	800	2400	Lot 7: 0/800 Lot 8: 0/800 Lot 9: 0/800	
EDR	B3	AEC-Q100-005	Specific tests and conditions to be defined in case of NVM	-	-	-	-	N/A (NVM not present into the component)

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

WBS	C1	AEC-Q100-001 AEC-Q003	Wire Bond Shear Test: (Cpk > 1.67)	30 bonds	5 parts Min.		All measurement within spec limits	Assembly data
WBP	C2	Mil-STD-883, Method 2011 AEC-Q003	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30 bonds	5 parts Min.		All measurement within spec limits	Assembly data
SD	C3	JESD22 B102 JSTD-002D	Solderability: (>95% coverage) 8hr steam aging prior to testing	1	15	15	All measurement within spec limits	Assembly data
D	C4	JESD22 B100, JESD22 B108 AEC-Q003	Physical Dimensions: (Cpk > 1.67)	3	10	30	All measurement within spec limits	Assembly data
SBS	C5	AEC-Q100-010 AEC-Q003	Solder Ball Shear: (Cpk > 1.67); 5 balls from min. of 10 devices	-	-	-	-	N/A (*only for BGA)*
LI	C6	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through- hole only; 10 leads from each of 5 devices	-	-	-	-	N/A (only for TTH)

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

EM	D1	JESD61	Data, test method and criteria should be available upon request	-	-	-	-	N/A
TDDB	D2	JESD35	Data, test method and criteria should be available upon request	-	-	-		N/A
HCI	D3	JESD60 & 28	Data, test method and criteria should be available upon request	-	-	-	-	N/A
NBTI	D4	JESD90	Data, test method and criteria should be available upon request	-	-	-		N/A
SM	D5	JESD61, 87, & 202	Data, test method and criteria should be available upon request	-	-	-	-	N/A

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)

TEST GROUP E - ELECTRICAL VERIFICATION

TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test: All parametric and functional tests	All	All	All	Applied	
HBM	E2	AEC-Q100-002	Target HBM=±4kV global pins vs GND, ±2kV all pins, ☐ Testing at Room ☐ Testing at Hot	-	-	-	-	N/A
CDM	E3	AEC-Q100-011	Target CDM=± 750V on corner pins; ± 500V all other pins ☐ Testing at Room ☐ Testing at Hot	-	-	-	-	N/A
LU	E4	AEC-Q100-004	Current Injection Class II - Level A (+/- 100mA) ☐ Testing at Room ☐ Testing at Hot	-	-	-	-	N/A
LU	E4	AEC-Q100-004	Overvoltage Class II - Level A (1,5 x Vmax) ☐ Testing at Room ☐ Testing at Hot	-	-	-	-	N/A
ED	E5	AEC-Q100-009 AEC-Q003	Electrical Distributions: (Test @ Rm/Hot/Cold) where applicable, Cpk >1.67)	3	30	90		passed
FG	E6	AEC-Q100-007	Fault Grading: FG shall be = or > 90% for qual units	-	-	-		N/A
CHAR	E7	AEC-Q003	Characterization: (Test @ Rm/Hot/Cold)	-	-	-		N/A
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	-	-	-		N/A for Fab transfer
SC	E10	AEC Q100-012	Short Circuit Characterization	-	-	-		N/A
SER	E11	JESD89-1 JESD89-2 JESD89-3	Applicable to devices with memory sizes 1Mbit SRAM or DRAM based cells. Either test option (un-accelerated or accelerated) can be performed, in accordance to the referenced specifications	-	-	-		N/A
LF	E12	AEC-Q005	Lead (Pb) Free: (see AEC-Q005)	-	-	-		Covered by Test group A & C

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)

TEST GROUP F – DEFECT SCREENING TESTS

PAT	F1	AEC-Q001	Process Average Testing: (see AEC-Q001)	All	All	All	Reject units outside Avg.	Not performed on qualification lots. It will be implemented starting from first production lot
SBA	F2	AEC-Q002	Statistical Bin/Yield Analysis: (see AEC-Q002)	All	All	All	Reject units outside criteria	Not performed on qualification lots. It will be implemented starting from first production lot

TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS
(for Ceramic Package testing only)

MS	G1	JESD22 B104	Mechanical Shock: (Test @ Rm)	-	-	-	-	N/A (for cavity package only
VFV	G2	JESD22 B103	Variable Frequency Vibration: (Test @ Rm)	-	-	-	-	N/A (for cavity package only
CA	G3	MIL-STD-883 Method 2001	Constant Acceleration: (Test @ Rm)	-	-	-	-	N/A (for cavity package only
GFL	G4	MIL-STD-883 Method 1014	Gross and Fine Leak:	-	-	-	-	N/A (for cavity package only
DROP	G5	----------	Drop Test: (Test @ Rm) MEMS cavity parts only. Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface.	-	-	-	-	N/A (for cavity package only
LT	G6	MIL-STD-883 Method 2004	Lid Torque:	-	-	-	-	N/A (for cavity package only
DS	G7	MIL-STD-883 Method 2019	Die Shear:	-	-	-	-	N/A (for cavity package only
IWV	G8	MIL-STD-883 Method 1018	Internal Water Vapor:	-	-	-	-	N/A (for cavity package only

Test	#	ST spec Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)

TEST GROUP H – ADDITIONAL RELIABILITY TESTS
(no Q100)

HTRB	4.4	0061692	Tj=150°C Duration= 1000 hrs ☒ Testing at Room ☒ Drift Analysis	1	45	45	Lot 1: 0/45	No significant drift observed in drift analysis

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PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/23/14096
1.3 Title of PCN	L9616-TR, L9616 (UB62): Assembly Transfer to Bouskoura
1.4 Product Category	L9616-TR, L9616
1.5 Issue date	2023-05-10

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	NEMETH KRISZTINA
2.1.2 Phone	+49 89460062210
2.1.3 Email	krisztina.nemeth@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Fabrizio CASSANI
2.1.2 Marketing Manager	Alberto CAROLI
2.1.3 Quality Manager	Alberto BIGNAZZI

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617)	ST Bouskoura - Morocco

4. Description of change		
	Old	New
4.1 Description	ST Shenzhen Assembly Plant	ST Bouskoura Assembly Plant
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No Impact	

5. Reason / motivation for change	
5.1 Motivation	Service and Capacity improvement. Manufacturing process optimization.
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	Dedicate Finished Good Codes

7. Timing / schedule	
7.1 Date of qualification results	2023-04-26
7.2 Intended start of delivery	2023-07-01
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	14096 Validation.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2023-05-10

9. Attachments (additional documentations)
14096 Public product.pdf 14096 Validation.pdf 14096 Details.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	L9616	

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