Dear Customer,

Following the continuous improvement of our service and in order to be ready to support the market demand of Power MOSFET Transistors, the products listed in the PCN will be manufactured in ASE-WEIHAI Subcontractor (China). PowerFLAT™ 8x8 HV devices produced ASE-WEIHAI (China), guarantee the same quality and electrical characteristics as reported in the relevant data sheets. Devices used for qualification are available as Samples.

The involved product series and affected packages are listed in the table below:

Product Family	Package	Commercial Product / Series
Power MOSFET Transistors	PowerFLAT™ 8x8 HV	STLxxxxxxx

Any other Product related to the above series, manufactured in PowerFLAT™ 8x8 HV Package, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 16-2015.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family Description	Part Number - Test Vehicle
Power MOSFET Transistors	STL19N60M2 STL57N65M5 STL23NM60ND

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability:

Product Family Description	1st Shipments
Power MOSFET Transistors	From Week 29-2015

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 days period will constitute acceptance of the change (Jedec Standard No. 46-C). In any case, first shipment may start earlier with customer written agreement.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of PowerFLAT™ 8x8 HV Package manufactured in ASE-WEIHAI (China), will be identified by 1st two digits of the traceability code are "GE". Furthermore, in order to benefit the advantage of the added driver source lead, please refer also to the suffix $V of internal code as reported in the Box Label of the packing.

Sincerely Yours.

FINAL Reliability Report

PowerFLAT™ 8x8 HV Back-End line relocation to ASE-WEIHAI (China)

General Information	
Product Lines:	MQ6G / M5FM / 2F67
Product Families:	Power MOSFET
P/Ns:	STL19N60M2 (MQ6G) STL57N65M5 (M5FM) STL23NM60ND (2F67)
Product Group:	IPG
Product division:	Power Transistor Division
Package:	PowerFLAT™ 8x8 HV
Silicon Process techn.:	MDmesh II™ (MQ6G) MDmesh™ V (M5FM) FDmesh™ II (2F67)

Locations	
Wafer Diffusion Plant:	Ang Mo Kio (Singapore) : MQ6G Catania: M5FM – 2F67
EWS Plant:	Ang Mo Kio (Singapore) Catania (Italy)
Assembly and testing plant:	ASE-WEIHAI (China)
Reliability Lab:	IPG-PTD Catania Reliability Lab.

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	February 2015	9	A.Settinieri	C. Cappello	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Reliability evaluation for PowerFLAT™ 8x8 HV ASE-WEIHAI (China)

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET

4.2 Construction note

D.U.T.: STL19N60M2 LINE: MQ6G PACKAGE: PowerFLAT™ 8x8 HV

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	MDmesh II™ Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	3950 x 3170 μm^2
Metal	AlSi
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ASE-WEIHAI (China)
Package description	PowerFLAT™ 8x8 HV
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	**Thermosonic**
Wires bonding materials	Cu 2mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*ASE-WEIHAI (China)*
Tester	**Statec**

D.U.T.: STL57N65M5 LINE: M5FM PACKAGE: PowerFLAT™ 8x8 HV

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania (Italy)
Technology	MDmesh™ V Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	7340 x 4750 μm^2
Metal	AlCu/Ti/TiN
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	*ASE-WEIHAI (China)*
Package description	PowerFLAT™ 8x8 HV
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	**Epoxy**
Die attach material	**Power Glue**
Wire bonding process	**Thermosonic**
Wires bonding materials	Cu 2 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*ASE-WEIHAI (China)*
Tester	**Statec**

D.U.T.: STL23NM60ND LINE: 2F67 PACKAGE: PowerFLAT™ 8x8 HV

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania (Italy)
Technology	FDmesh™ II Power MOSFET
Die finishing back side	**Ti/Ni/Ag**
Die size	5620 x 4600 μm^2
Metal	AlSi
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	*ASE-WEIHAI (China)*
Package description	PowerFLAT™ 8x8 HV
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	**Epoxy**
Die attach material	**Power Glue**
Wire bonding process	**Thermosonic**
Wires bonding materials	Cu 2mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*ASE-WEIHAI (China)*
Tester	**Statec**

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	line	Tech.	package	Comments
1	MQ6G	MDmesh II™	PowerFLAT™ 8x8 HV	Power MOSFET HV
2	M5FM	MDmesh™ V		
3	2F67	FDmesh™ II		

5.2 Reliability test plan summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			
						MQ6G	**M5FM**	**2F67**	*NOTE*
Die Oriented Tests									
TEST			All qualification parts tested per the requirements of the appropriate device spec.			235	235	235	
External Visual			All devices submitted for testing			235	235	235	
HTRB	**N**	**JESD22 A-108**	**TA = 150°C BIAS (480V) MQ6G / 2F67 BIAS (520V) M5FM**	135	168 H	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	
HTFB	**N**	**JESD22 A-108**	**TA = 150°C BIAS = 30V**	135	168 H	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	
HTSL	**N**	**JESD22 A-103**	**TA = 150°C**	135	168 H	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	
PC		**JESD22 A-113**	**Drying 24 H @ 125°C Store 168 H @ TA=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times**	All devices to be subjected to H3TRB, TC, AC		pass	pass	pass	*Pcs mounted on card-edge*
AC	**Y**	**JESD22 A-102**	**Pa=2Atm / TA=121°C**	75	96 H	0/25	0/25	0/25	
TC	**Y**	**JESD22 A-104**	**TA = -65°C to 150°C**	75	100 cy	0/25	0/25	0/25	
					200 cy	0/25	0/25	0/25	
					500 cy	0/25	0/25	0/25	
H3TRB	**Y**	**JESD22 A-101**	**TA=85°C , RH=85% , BIAS= 100V**	75	168 H	0/25	0/25	0/25	
					500 H	0/25	0/25	0/25	
					1000 H	0/25	0/25	0/25	
IOL / TF	**N**	**MIL-STD-750 Method 1037**	**ΔTC=105°C**	75	10Kcy	0/25	0/25	0/25	

6 ANNEXES 6.0

6.1 Tests Description

Test name	Description	Purpose
Die Oriented Tests		
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max.operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented Tests		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	To verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

PowerFLAT™ 8x8 HV Schematic Diagram CARSEM vs ASE-WEIHAI

S(4) Bottom view
S(3)
S(2)
G(1)
D(3)

Drain D(3)
Gate G(1)
Power source S(2)≡S(3)≡S(4)

Internal Schematic A

CARSEM (Malaysia)

Drain D(3)
Gate G(1)
Driver source S(2)
Power source S(3)≡S(4)

Internal Schematic B (1)

ASE-WEIHAI (China)

Advantage of the added driver source lead

The introduction of the fourth (driving) pin strongly improves the dynamic performance of Power MOSFET devices, which is even more evident when the switching current levels and the output power levels are higher during both device turn-off and turn-on.