PRODUCT/PROCESS CHANGE NOTIFICATION

TITLE	**H2PAK (LV MOSFET) - Assy Flow Optimization**
IMPACTED PRODUCTS	LV MOSFET in H2PAK: see list
MANUFACT. STEP	Assembly
INVOLVED PLANT	ST Shenzhen – China
CHANGE REASON	Quality Improvement
CHANGE DESCRIPTION	New assembly flow on H2PAK package moving from one step crop (exposed copper area in dambar cut zone) to dual step crop (leads fully plated – no exposed copper) See below details
TRACEABILITY	Dedicated Finished Good Codes
VALIDATION	According to ZVEI recommendations: x SEM-PA-17 — Change of specified-assembly process sequence (deletion and/or additional process step) x SEM-EQ-02 — Production from a new equipment/tool which uses the same basic technology (replacement equipment or extension of existing equipment pool) without change of process.
REPORTS	Qualification report is enclosed to this Notification 14004 Validation.pdf

New assembly flow qualification on H2PAK package in ST Shenzhen plant moving from one step crop to dual step crop.

Agenda

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Change description

- Aim of this document is to describe the activity performed to qualify the new assembly flow on H2PAK package moving from one step crop (exposed copper area in dambar cut zone) to dual step crop (leads fully plated – no exposed copper).
- The H2PAK package is assembled in STMicroelectronics Shenzhen plant.
- Detailed qualification activity has been performed in order to qualify the new assembly flow for H2PAK package.
- This report shows the positive results achieved. The new flow is ensuring the improvement of leads plating quality leaving unchanged the product electrical characteristics.
- All reliability tests have been completed with positive results.

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ZVEI Guidelines

- According to ZVEI recommendations, the notification is required.

Mark change	ID	Type of change	Assessment of impact on Supply Chain regarding following aspects - contractual agreements - technical interface of processability/manufacturability of customer - form, fit, function, quality performance, reliability		Remaining risks within Supply Chain?	Understanding of semiconductors experts	Examples to explain	A: Application level B: Boardlevel C: Component level *: Not relevant for qualification matrix
			No	Yes				
x	SEM-PA-17	Change of specified-assembly process sequence (deletion and/or additional process step)	--	P	**(--):** no influence in final product integrity or *specified sequence* **(P):** influence in final product integrity or *specified sequence*	**(--):** e.g. additional cleaning step e.g. deletion of optical inspection **(P):** e.g. change lead finishing pre trim & form to post trim & form	C	
x	SEM-EQ-02	Production from a new equipment/tool which uses the same basic technology (replacement equipment or extension of existing equipment pool) without change of process.	--	P	PCN required for dedicated equipment for sensitive component production. **(--):** If change does not influence the integrity of the final product. **(P):** If impact on product integrity is anticipated.	**(--):** e.g. extension of existing equipment pool **(P):** e.g. extension of dedicated equipment in case basic technology still need to be proven	C	

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Selected Test Vehicles & impacted products list

TVs LINE DEVICE	TVs COMMERCIAL PROD
OD0J01	STH240N10F7-6
OD0KA1	STH315N10F7-6
OD8L01	STH270N8F7-6

LINE DEVICE	COMMERCIAL PROD
4D7K01	STH240N75F3-6
4L2KA1	STH300NH02L-6
6D4KA1	STH320N4F6-6
OD0J01	STH240N10F7-6
OD0K01	STH310N10F7-6
OD0KA1	STH315N10F7-6
OD4KA1	STH410N4F7-6AG
OD4KA1	STH410N4F7-6HT
OD8L01	STH270N8F7-6
OD8LA1	STH275N8F7-6AG

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Assembly Flow Comparison

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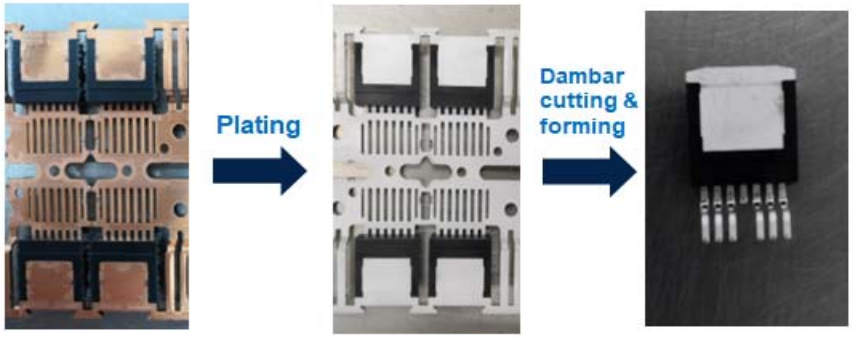
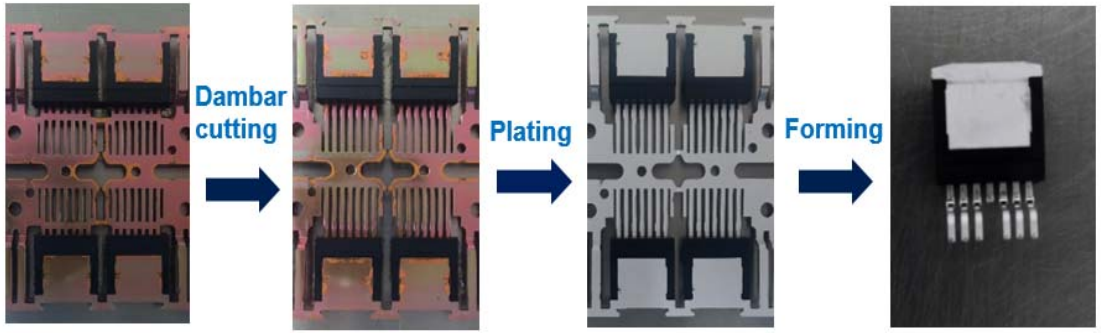
Process line description

To eliminate exposed copper area in dambar cut zone, firstly proceed dambar cutting and then plating and forming.

Actual line process



New line process



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Conclusions

- Detailed qualification activity has been performed in order to qualify the new assembly flow on H2PAK package in STMicroelectronics Shenzhen moving from one step crop (exposed copper area in dambar cut zone) to dual step crop (leads fully plated – no exposed copper).
- All reliability tests have been completed with positive results (see attached reliability report).
- Neither functional nor parametric rejects were detected at final electrical test.
- The new flow is ensuring the improvement of leads plating quality leaving unchanged the product electrical characteristics.

RELIABILITY EVALUATION REPORT

Cropping process change for H2PAK 6/7L packages in ST SHENZHEN(China)

General Information	Traceability
Commercial Product: STH270N8F7-6	Diffusion Plant: Singapore SG8
Product Line: OD8L	Assembly Plant: Shenzhen
Product Description: LVMOS	Reliability Lab: Shenzhen
Package: H2PAK	Passed
Silicon Technology: PMOSFET OFT1	

General Information	Traceability
Commercial Product:STH315N10F7-6	Diffusion Plant: Catania CTM8
Product Line: OD0k	Assembly Plant: Shenzhen
Product Description: LVMOS	Reliability Lab: Shenzhen
Package: H2PAK	Passed
Silicon Technology: PMOSFET OFT1	

General Information	Traceability
Commercial Product:STH240N10F7-6	Diffusion Plant: Singapore SG8
Product Line: OD0J	Assembly Plant: Shenzhen
Product Description: LVMOS	Reliability Lab: Shenzhen
Package: H2PAK	Passed
Silicon Technology: PMOSFET OFT1	

Revision history

Rev.	Changes description	Author	Date
1.0	Cropping process change for H2PAK 6/7L	Jian GUO	2023-02

Approved by

Function	Location	Name	Date

TABLE OF CONTENTS

1. Reliability Evaluation Overview

1.1. Objective

Aim of this report is to present the results of the reliability evaluations performed on process change to release the new process for H2PAK 6/7L in production in H2PAK package in ST Shenzhen (China).

The process change is apply to eliminate Tin burr issue.

1.2. Reliability Strategy and Test Plan

1.2.1. Reliability strategy

Reliability trials performed as part of this reliability evaluation are in agreement with ST 0061692 and AEC-Q101 rev E specification, as below Test Plan. For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

1.2.2. Test Plan

#	Stress	Abrv	Reference	Data type	Comments
1	Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	Y	
2	External Visual	EV	JESD22B-101	Y	
3	Pre-conditioning	PC	JESD22A-113	Y	
4	Temperature Cycling	TC	JESD22A-104	Y	
5	Environmental Sequence	ES	DMS 0061692 Annex1	Y	

1.3. Conclusion

All reliability testes have been completed with positive results. Neither electrical nor parametric rejects were detected at final electrical testing.

The CSAM and TSAM result are acceptable for H2PAK.

2. Product Characteristics

2.1. Generalities

2.1.1. Test vehicle

STH270N8F7-6(R2(4*OD8L8B2)

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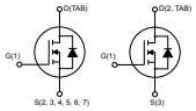
STH270N8F7-2, STH270N8F7-6, STP270N8F7

Datasheet

N-channel 80 V, 0.0017 Ω typ., 180 A STripFET F7 Power MOSFETs in an H²PAK-2, H²PAK-6 and TO-220 packages



H²PAK-2, H²PAK-6 TO-220

Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D
STH270N8F7-2	80 V	0.0021 Ω	180 A
STH270N8F7-6			
STP270N8F7		0.0025 Ω	

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

These N-channel Power MOSFETs utilize STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

STPOWER

Product status links
STH270N8F7-2
STH270N8F7-6
STP270N8F7

STH315N10F7-6(R2(4*OD0K5A3)

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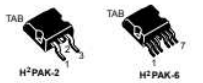
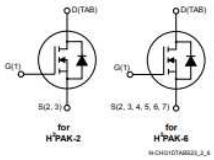
STH315N10F7-2, STH315N10F7-6

Datasheet

Automotive-grade N-channel 100 V, 2.1 mΩ typ., 180 A STripFET F7 Power MOSFETs in an H²PAK-2 and H²PAK-6 packages





Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STH315N10F7-2	100 V	2.3 mΩ	180 A
STH315N10F7-6			

- AEC-Q101 qualified
- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

These N-channel Power MOSFETs utilize STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status
STH315N10F7-2
STH315N10F7-6

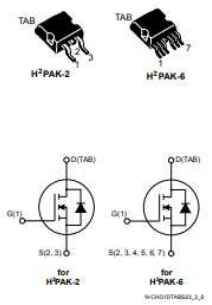
Product summary	
Order code	STH315N10F7-2
Marking	315N10F7
Package	H²PAK-2
Packing	Tape and reel
Order code	STH315N10F7-6
Marking	315N10F7
Package	H²PAK-6
Packing	Tape and reel

STH240N10F7-6 (R2(4*OD0J8B2)

STH240N10F7-2, STH240N10F7-6

Datasheet

N-channel 100 V, 2 mΩ typ., 180 A STripFET™ F7 Power MOSFETs in an H²PAK-2 and H²PAK-6 packages



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STH240N10F7-2	100 V	2.5 mΩ	180 A
STH240N10F7-6			

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Description

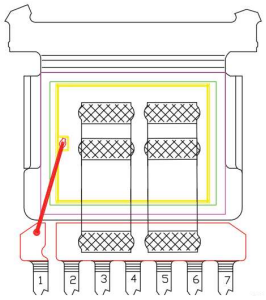
These N-channel Power MOSFETs utilize STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status
STH240N10F7-2
STH240N10F7-6

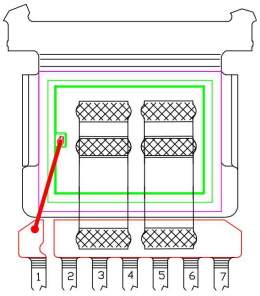
Product summary	
Order code	STH240N10F7-2
Marking	240N10F7
Package	H²PAK-2
Packing	Tape and reel
Order code	STH240N10F7-6
Marking	240N10F7
Package	H²PAK-6
Packing	Tape and reel

2.2. Pin connection/bonding diagram

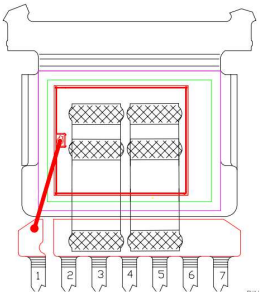
OD8L



OD0K



OD0J



2.3. Traceability

2.3.1. Wafer information

Wafer fab information_OD8L	
Wafer fab name / location	Singapore
Wafer diameter (inches)	8"
Silicon process technology	PMOSFET OFT1
Die finishing front side	NO PASSIVATION
Die finishing back side	Ti-NiV-Ag
Die size (micron)	6340 x 4900
Metal levels/ materials/ thicknesses	Ti/TiN/TiAlCu 6.0um

Wafer fab information_OD0K	
Wafer fab name / location	Catania
Wafer diameter (inches)	8"
Silicon process technology	PMOSFET OFT1
Die finishing front side	TEOS/NITRIDE
Die finishing back side	Ti-NiV-Ag
Die size (micron)	6340 x 4600
Metal levels/ materials/ thicknesses	AlCu/Ti/TiN 6.1um

Wafer fab information_OD0J	
Wafer fab name / location	Singapore
Wafer diameter (inches)	8"
Silicon process technology	PMOSFET OFT1
Die finishing front side	NO PASSIVATION
Die finishing back side	Ti-NiV-Ag
Die size (micron)	5600 x 4590
Metal levels/ materials/ thicknesses	Ti/TiN/TiAlCu 4.5um

2.3.2. Assembly information

Assembly information_OD8L & OD0K & OD0J	
Assembly plant name / location	ST SHENZHEN (China)
Package description	D2PAK
Lead frame/Substrate	5FT86729
Die attach material	PREFORM Pb/Ag/Sn 95.5/2.5/2
Wire bonding material/diameter	RIBBON Al 80x10mils - WIRE Al-Mg D5
Molding compound material	RESIN SUMITOMO EME7026
Package Moisture Sensitivity Level (JEDEC J-STD020D)	Moisture Sensitivity 1 (UNLIMITED at <=30C/85%RH)

2.3.3. Reliability Testing information

Reliability laboratory location	ST SHENZHEN (China)

3. Tests Results Summary

3.1. Lot Information

Lot#	Commercial product	RL code	Diffusion Lot	Trace Code
Lot1	STH270N8F7-6	R2(4*OD8L8B2	VC0496E7	GK21418K
Lot2	STH315N10F7-6	R2(4*OD0K5A3	V5122MXN	GK214144
Lot3	STH240N10F7-6	R2(4*OD0J8B2	VC20510X	GK2140P1

3.2. Test results summary

No	Test Name	Reference	Condition/ Method	Steps	Failure/SS		
					Lot 1	lot 2	lot 3
1	TEST	User specification	All qualification parts tested per the requirements of the appropriate device specification.		0/2000	0/2000	0/2000
2	EV	JESD22 B-101	All devices submitted for testing		0/2000	0/2000	0/2000
3	PC	JESD22A-113	Bake 24 hrs@ 125° C Soak 192 hrs@ 30° C / 60% RH Reflow Profile =J-STD-020D(Tmax= 260°C)	ATE	0/154	0/154	0/154
				TSAM	0/40	0/40	0/40
				CSAM DIE/LEAD	0/40	0/40	0/40
4	TC	JESD22A-104	TA =-65°C / +150° C 1000cycle	ATE	0/77	0/77	0/77
				TSAM	0/20	0/20	0/20
				CSAM DIE/LEAD	0/20	0/20	0/20
5	EnvSeq	DMS 0061692 Annex1	TA =-65°C / +150° C 100cycle PPT 96hrs@121°C/ 2Atm	ATE	0/77	0/77	0/77
				TSAM	0/20	0/20	0/20
				CSAM DIE/LEAD	0/20	0/20	0/20