PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-PWR/11/6183
Notification Date 01/25/2011

Continuous improvement by upgrading the top metal barrier of 50V RF DMOS technologies from TiTiONTi to TiW

Table 1. Change Implementation Schedule

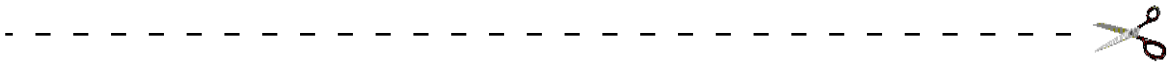
Forecasted implementation date for change	01-Jun-2011
Forecasted availabillity date of samples for customer	18-Jan-2011
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	18-Jan-2011
Estimated date of changed product first shipment	01-Oct-2011

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	STAC2932B/F and SD293x family - see attached list
Type of change	Waferfab process change
Reason for change	to reduce the risk of gold contamination
Description of the change	In order to reduce the risk of gold contamination that may affect sensitive products sourced from the 6" wafer fab located in ST Catania, Italy, it has been requested by ST Quality Management to avoid Gold back-sputtering in the etcher chamber;we will soon change the top metal barrier of our 50V RF DMOS technologies. The change includes the modification of the top metal barrier from TiTiONTi to TiW guaranteeing at least the same quality and electrical characteristics as those reported in the relevant datasheets and documents. Samples with new TiW barrier from qualification lots are now available upon request.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	See the W at the end of CP and marked on the package
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN APM-PWR/11/6183**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 01/25/2011**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Juhel, Serge	Division Marketing Manager
Di giovanni, Filippo	Division Product Manager
Calderoni, Michele	Division Q.A. Manager

RELIABILITY REPORT

PROCESS CHANGE

SD2931-10

General Information	
Product Line	*1931*
Product Description	*SD2931-10*
Product Group	*IMS-APM*
Product division	*Power RF - DMOS*
Package	*M174*
Silicon Process technology	*DMOS-LV*

Locations	
Wafer fab	*CT 6" LIP*
Assembly plant	*ST – Bouskoura*
Reliability Lab	*CATANIA – Rel. Lab*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	Nov-2010	6	Ivan De Luca	Giovanni Presti	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Due to Gold contamination sensitive products mix in today 6" wafer fab located in ST Catania – Italy, it has been requested by ST Quality Management, to avoid Gold back-sputtering in the etcher chamber.

As a result of the above, in an effort to guarantee a better equipment rationalization and continuously improve process and product quality, the top metal barrier of our 50V RF DMOS technologies has been changed. The change includes the modification of the top metal barrier from TiTiONTi to TiW guaranteeing at least the same quality and electrical characteristics.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The SD2931-10 is a gold metallized N-Channel MOS field-effect RF power transistor. It is intended for use in 50 V dc large signal applications up to 230 MHz.

4.2 Construction note

P/N = SD2931-10	Lot1= Y004015A, Lot2= Y938211 , Lot3= Y004015B
Wafer/Die fab. information	
Wafer fab manufacturing location	CT 6" LIP
Technology	DMOS-LV
Process family	DMOS
Die finishing back side	AuAs
Die size	5380 x 3260 um^2
Bond pad metallization layers	Au
Passivation type	OXNITRIDE
Poly silicon layers	YES (6000 Ang)
Intermediate dielectric	PVAPOX (10 KÅ)
Barrier Layer	TiW
Wafer Testing (EWS) information	
Electrical testing manufacturing location	CATANIA
Tester	TESEC
Assembly information	
Assembly site	ST – Bouskoura
Package description	M174
Die attach process	Hard
Die attach material	Au eutectic
Die pad size	80*150 um^2
Wire bonding process	Wedge wire bonding technology
Wires bonding materials/diameters	Au / 2 mils
Final testing information	
Testing location	ST – Bouskoura - CASABLANCA
Tester	TESEC

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Process/ Package	Product Line	Comments
1	Y004015A	M174	1931	
2	Y938211	M174	1931	
3	Y004015B	M174	1931	

5.2 Test plan and results summary

P/N: SD2931-10

Test		Std ref.	Conditions	SS	Steps	Failure/SS			Notes
						Lot 1	Lot 2	Lot3	
HTRB		JESD22 A-108	Tj = 175℃, Vdd= 100V	144	168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	
HTFB		JESD22 A-108	Tj = 175℃, Vgg= 20V	144	168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	
HTSL		JESD22 A-103	Ta = 200℃	160	168 H	0/45			
					500 H	0/45			
					1000 H	0/45			
TC		JESD22 A-104	Ta = -65 to 150℃	150	100 CY	0/77	0/77	0/77	
					200 CY	0/77	0/77	0/77	
					500 CY	0/77	0/77	0/77	

6 ANNEXES

6.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

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