Reliability Report

General Information	
Product Line	*U337*
Product Description	*Combo IC for PFC and ballast control*
Product division	*I&PC*
Package	*SO20*
Silicon process technology	*BCD OFFLINE*

Locations	
Wafer fab location	*ANG MO KIO*
Assembly plant location	*MUAR*
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	6-Apr-18	13	G. Capodici	Original document

Approved by
A. Paratore

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
0061692	: Reliability tests and criteria for qualifications

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of U337 device diffused in ANG MO KIO and assembled in SO20 in MUAR in the overall plan of the new SOIC20L IDF L/F project with new BOM qualification.

According to Reliability Qualification Plan, below is the list of the trials performed:

Die Oriented Tests
- High Temperature Operating Life
- High Temperature Reverse Bias

Package Oriented Tests
- Preconditioning
- Temperature Cycling
- Autoclave
- High Temperature Storage Life
- Temperature Humidity Bias

Electrical Characterization
- ESD resistance test

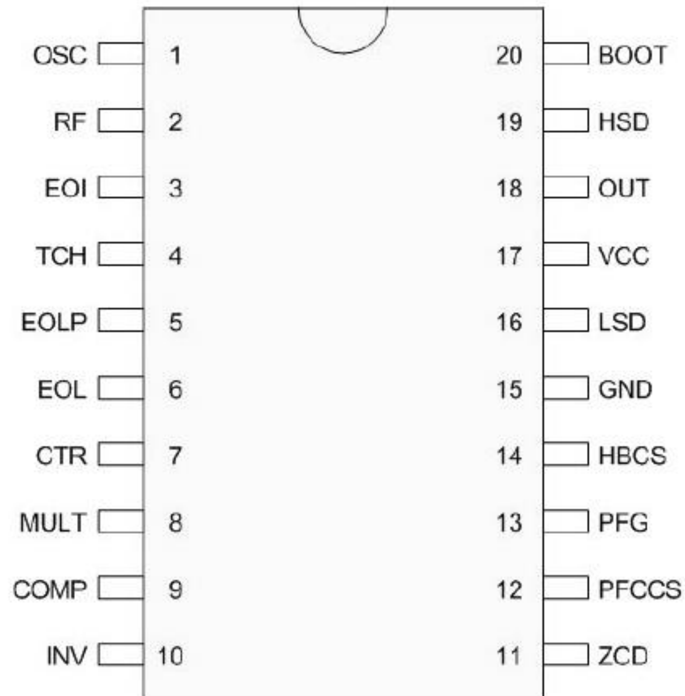
2.2 Conclusion

Taking in account the results of the trials performed **the U337 diffused in ANG MO KIO and assembled in SO20 in MUAR** has positively passed reliability evaluation.

3 DEVICE CHARACTERISTICS

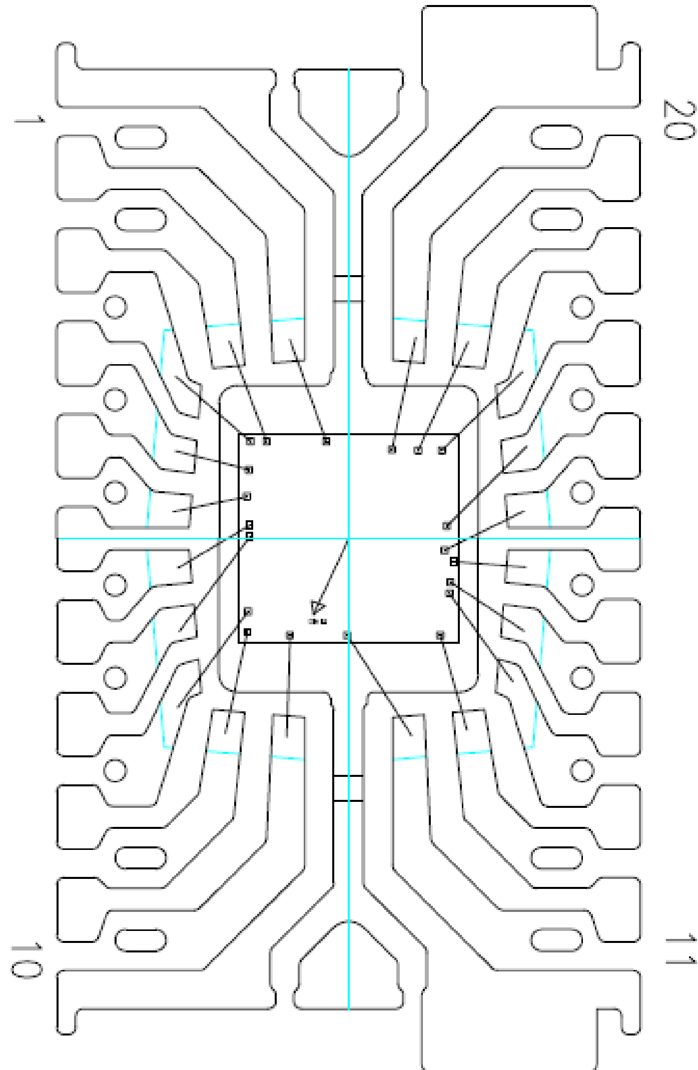
3.1 Device description

3.1.1 Pin connection



3.1.2 Bonding diagram

FRAME PAD : 0.140 x 0.165 Inch
3560 x 4200 um



3.2 Traceability

Wafer fab information	
Wafer fab manufacturing location	*ANG MO KIO*
Wafer diameter	*6 inches*
Wafer thickness	*375 µm*
Silicon process technology	*BCD Offline*
Die finishing back side	*Cr/Ni/Au*
Die size	*3170x3025 µm*
Bond pad metallization layers	*AlSiCu*
Passivation	*SiN*
Metal levels	*1*

Assembly Information	
Assembly plant location	*MUAR*
Package description	*SO20*
Die pad size	*3.56x4.2 mm*
Molding compound	*EME-G633*
Wires bonding materials/diameters	*Au/1mil*
Die attach material	*ABP 8302*
Lead solder material	*Sn*

4 TESTS RESULTS SUMMARY

4.1 LOTs information

Lot ID #	Silicon Rev.	Package	Assy Plant	Diff. Plant	Comments
1	AB6	SO20W	MUAR	ANG MO KIO	IDF – new BOM
2	AB6	SO20W	MUAR	ANG MO KIO	Standard ver.

4.2 Test plan and results summary

Die Oriented Tests							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			Lot 1	**Lot 2**	**Lot 3**		
HTRB	High Temperature Reverse Bias						
		Conditions: Vcc=17V Tj=150°C	**0/77**	**0/22**	-	**1000h**	
HTOL	High Temperature Operating Life						
	PC before	**Conditions: Vcc=16V Tj=150°C**	**0/77**	**0/77**	-	**1000h**	

Package Oriented Tests							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			Lot 1	**Lot 2**	**Lot 3**		
PC	Pre-Conditioning: Moisture sensitivity level 3						
		192h 30°C/60% - 3 reflow PBT 260°C	**0/210**	**0/77**	-		
THB	Temperature Humidity Bias						
	PC before	**Ta=85°C/85%RH**	**0/77**	-	-	**1000h**	
AC	Autoclave						
	PC before	**121°C 2atm**	**0/77**	-	-	**96h**	
TC	Temperature Cycling						
	PC before	**Temp. range: -65/+150°C**	**0/77**	-	-	**500cy**	
HTSL	High Temperature Storage						
	No bias	**Tamb=150°C**	**0/77**	-	-	**1000h**	

Electrical Characterization Tests							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			Lot 1	**Lot 2**	**Lot 3**		
ESD	Electro Static Discharge						
	Human Body Model	**+/- 2kV (900V for HV pins)**	-	**0/3**	-		
	Machine Model	**+/- 125V (100V for HV pins)**	-	**0/3**	-		
	Charge Device Model	**+/- 500V (750V on corner pins)**	**0/3**	**0/3**	-		
LU	Latch-Up						
	Over-voltage and Current Injection	**Tamb=85°C Jedec78**	-	**0/6**	-		

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

5.1.2 High Temperature Reverse Bias

This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs @ Ta=25°C
- Final Testing @ 1000hrs @ Ta=25°C

5.2 Package oriented tests

5.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance.
The typical failure modes are "pop corn" effect and delamination.

5.2.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.2.3 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 200 cycles.
- Final Testing @ 500 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -65°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.2.4 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (96hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 96 hrs

5.2.5 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 1000 h.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs
- Final Testing (1000 hr.) @ Ta=25°C

5.3 Electrical Characterization Tests

5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less
IN high	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less

5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** JEDEC STANDARD JESD22-A114
  CDF-AEC-Q100-002
- **Machine Model** JEDEC STANDARD EIA/JESD-A115
  CDF-AEC-Q100-003
- **Charge Device Model** ANSI/ESDA/JEDEC JS002
  CDF-AEC-Q100-011

Reliability Qualification Report

ST Muar PowerSO 20 Genealogy creation for product with PowerSO-20/30 and New BOM Assessment

General Information	
Product Line	XUR15AJ6
Product Code	I6Z7*UR15AJ6
Product From	L6205D-3LF/
Product Description	DMOS DUAL FULL BRIDGE DRIVER (motor control applications)
Package Technology	SO 20 .30 TO JEDEC MS-013

Locations	
Wafer Fab Location	AM6F - Singapore 6"
Assembly Plant Location	MU1A ST MUAR - MALAYSIA
Testing Plant	MU1T ST MUAR - MALAYSIA
Reliability Assessment	QA REL LAB ST MUAR - MALAYSIA

Issued By: Mohd Ibrahim GHAZALI

Approved By: Francesco VENTURA

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document Reference	Short Description
AEC-Q100	Stress test qualification for integrated circuits
SOP 2.6.11	Project management for product development
SOP 2.6.19	Front-end technology platform development & qualification
SOP 2.6.2	Internals change management
SOP 2.6.7	Product maturity level
SOP 2.6.9	Package and process maturity management in Back End
SOP 2.7.5	Automotive products definition and status
0061692	Reliability tests and criteria for product qualification
8160601	Internal reliability evaluation report template
8161393	General specification for product development
7512807	Delamination analysis for plastic packages in reliability

2 TEST GLOSSARY

TEST NAME	DESCRIPTION
PC (JL3)	Preconditioning (Solder Simulation)
TC	Temperature Cycling
AC or PPT	Autoclave or Pressure Pot Test
HTSL	High Temperature Storage Life

life.augmented

RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

This report contains the reliability evaluation of UR15 device diffused in ANG MO KIO and assembled in SO20 in MUAR in the overall plan of the new SOIC20L IDF L/F project with new BOM qualification.

The main objective for this trial is to convert existing BOM to the new BOM .
For the reliability assessment evaluation the following stress test were carried out:

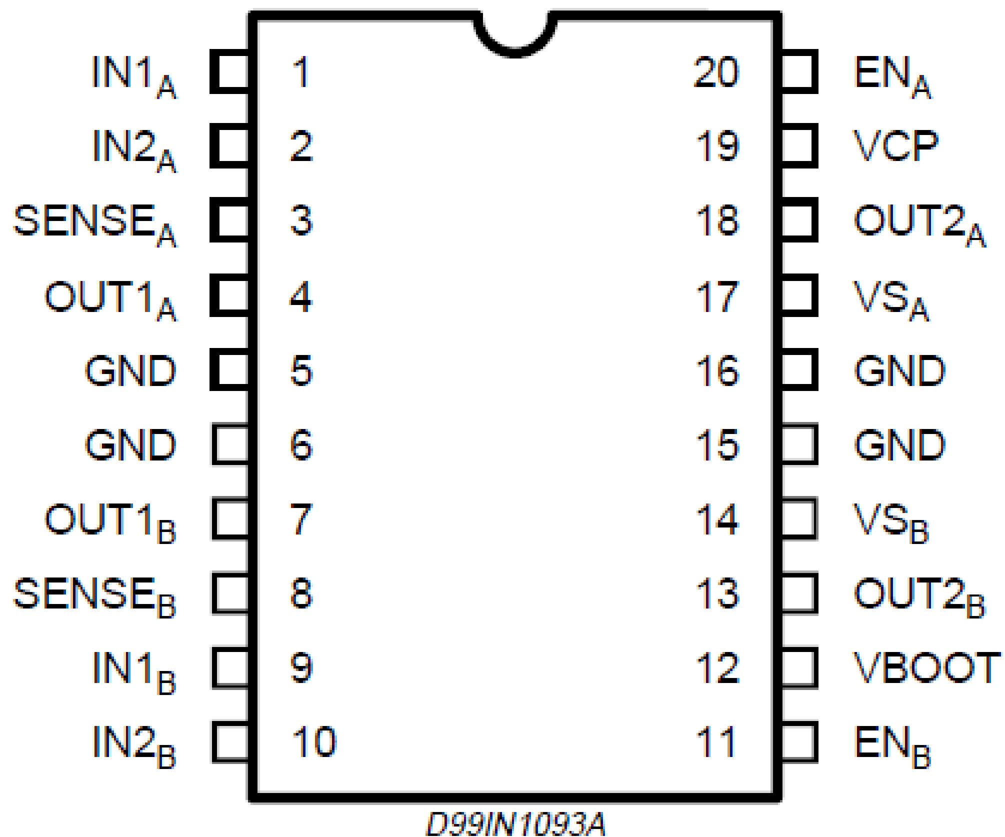
- Preconditioning JL3 (3X Reflow)
- Thermal Cycle Test (TCT)
- Autoclave / Pressure Pot Test (PPT)
- High Temperature Storage Life (HTSL)

3.2 Conclusions

All reliability tests have been completed with positive results. Package oriented test and destructive physical analysis (SAM) also have not put in evidence any criticality to package robustness.

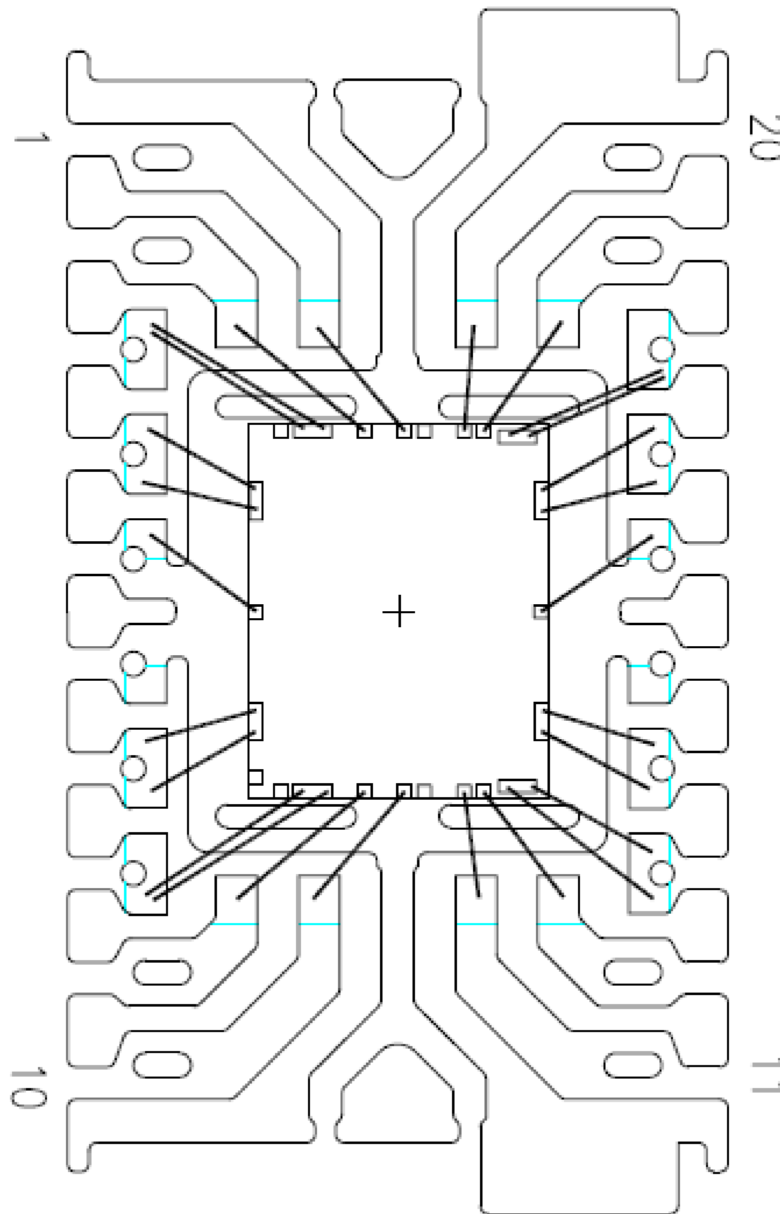
4.1 Device Description

4.1.1 Pin Connection



4.1.2 Bonding Diagram

FRAME PAD : $\frac{0.200 \times 0.230 \text{ inch}}{5.080 \times 5.840 \text{ mm}}$



4.2 Traceability

Wafer Fab Information	
Wafer fab manufacturing location	AM6F - Singapore 6"
Wafer diameter	6 inch
Wafer thickness	375 +/-25 UM
Silicon process technology	BCD3S
Die finishing back side	CHROMIUM /NICKEL / GOLD
Die finishing front side	USG-PSG-SiON-PIX
Die Size	3570,4550 UM
Bond pad metallization layers	AlSiCu
Passivation	SiN
No of Metal Layer	3

Assembly Information	
Assembly plant location	MU1A ST MUAR - MALAYSIA
Package description	SO 20 .30 TO JEDEC
Molding compound	EME-G633CA
Wire bonding materials/diameters	Au 1.5mils
Die attach material	ABP8302
Lead frame material	FRAME SO 20L 200x230
Lead solder material	Sn

Final Testing Information	
Electrical testing location	Plant MU1T ST MUAR - MALAYSIA
Tester	A565

5. TEST RESULTS SUMMARY

5.1 Lot Information

Lot #	Diffusion Lot	Lot Details / Trace Code	Assy Lot Id	Testing Lot Id
1	V6648J3T	997150Q705 (NEW BOM)	997150Q705	997150Q705

5.2 Test Plan and Results Summary (Electrical Test)

Reliability Test Status						
No	Test Name	Prec.	Condition/ Method	Steps	Fails/SS	Notes
					Lot 1	
1	PC (JL3)		Bake 24hrs @ 125°C Soak 192hrs @ 30°C/60%RH Reflow Profile = J-STD-020D (Peak Tmax = 260°C)	Final	0 / 350	Pass
2	TC	Yes	Test Conditions = -65°C / +150°C	500cyc	0 / 77	Pass
				1000cyc	0 / 77	Pass
3	AC	Yes	Test Conditions = Ta = 121°C / 2 ATM	96hrs	0 / 77	Pass
				168hrs	0 / 77	Pass
4	HTSL	No	Test Conditions = Ta = 150°C (without Bias)	500hrs	0 / 77	Pass
				1000hrs	0 / 77	Pass

NOTES

All units electrically tested good after each reliability test readout.

5.3 Test Plan and Results Summary (SAM Analysis)

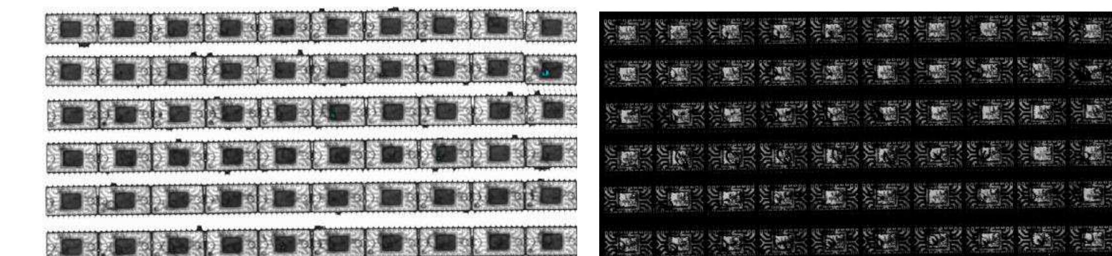
Reliability Test Status						
No	Test Name	Prec.	Condition/ Method	Steps	Fails/SS	Notes
					Lot 1	
1	PC (JL3)		Bake 24hrs @ 125°C Soak 192hrs @ 30°C/60%RH Reflow Profile = J-STD-020D (Peak Tmax = 260°C)	Final	0 / 40	No Delam
2	TC	Yes	Test Conditions = -65°C / +150°C	500cyc	0 / 20	No Delam
				1000cyc	0 / 20	No Delam
3	AC	Yes	Test Conditions = Ta = 121°C / 2 ATM	96hrs	0 / 20	No Delam
				168hrs	0 / 20	No Delam
4	HTSL	No	Test Conditions = Ta = 150°C (without Bias)	500hrs	0 / 20	No Delam
				1000hrs	0 / 20	No Delam

NOTES

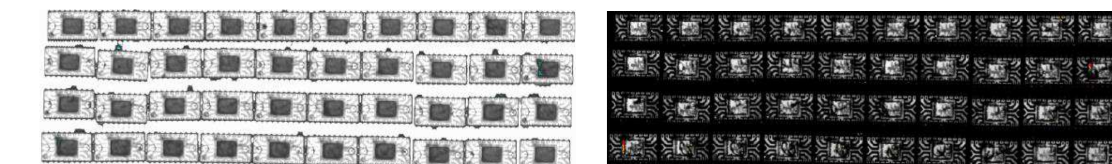
No any delamination issue on Die Attach Material (DAM) & also on Die / Molding Compound (Die Top).

5.3.1 SAM IMAGES

Time-0 (Before Preconditioning)



After Preconditioning (MSL3 & 3X Reflow)



6. TESTS DESCRIPTION

6.1 Package tests description

TEST NAME	DESCRIPTION	PURPOSE
PC (JL3) Preconditioning MSL3 (solder simulation)	The device is submitted to a typical temperature profile used for surface mounting after storage in a control moisture absorption.	As stand-alone test: to investigate the level of moisture sensitivity. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are link to metal displacement, dielectric cracking, molding compound delamination, wire bonds failure, die crack.
AC or PPT Autoclave / Pressure Pot Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. To point out critical water entry paths with consequent electrochemical and galvanic corrosion.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max temperature allowed by the package materials, sometimes higher than the max operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding